



Towards all-solution processable transistors and switches: plotter-printing of electrodes and spray-deposition of a semiconductor

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ABSTRACT

Organic electronic devices, like field-effect transistors (FETs) or switches, have received extensive attention because of their potential application in flexible electronics, large-area displays, radio-frequency identification tags (RFIDs), sensors, etc. Crucial advantage of organic electronics rests in a prospect of low cost manufacturing of electronic circuits achievable by deposition of electronic components from solution by, e.g., ink-jet printing and spray coating. The printing is desirable in the case of fine structures like interdigitated electrodes while spray brushing is more effective for fabrication of large area thin films.

A common challenge in most printing techniques is the limitation in feature size. The linewidth of 20-100 μm is achievable with standard ink-jet printers. The size of printed features may be decreased down to a few microns using laser-assisted technique at the price, however, of a dramatic increase of the cost of fabrication [1]. One of the ways of obtaining small-size features of printed elements may be paved by plotter printing. Advantage of the plotting technique is possibility of drawing very smooth lines enabling one to achieve short (ca. 5 μm) channel between source and drain electrodes. On the other hand, this method is not contactless, thus limiting the choice of materials for substrates [2]. Spray deposition of semiconductor/dielectric/metallic layers building an electronic device is less sensitive to solution properties (e.g. viscosity) in comparison to ink-jet printing and, contrary to the spin coating technique, allows for a successive deposition of several layers using the same solvent.

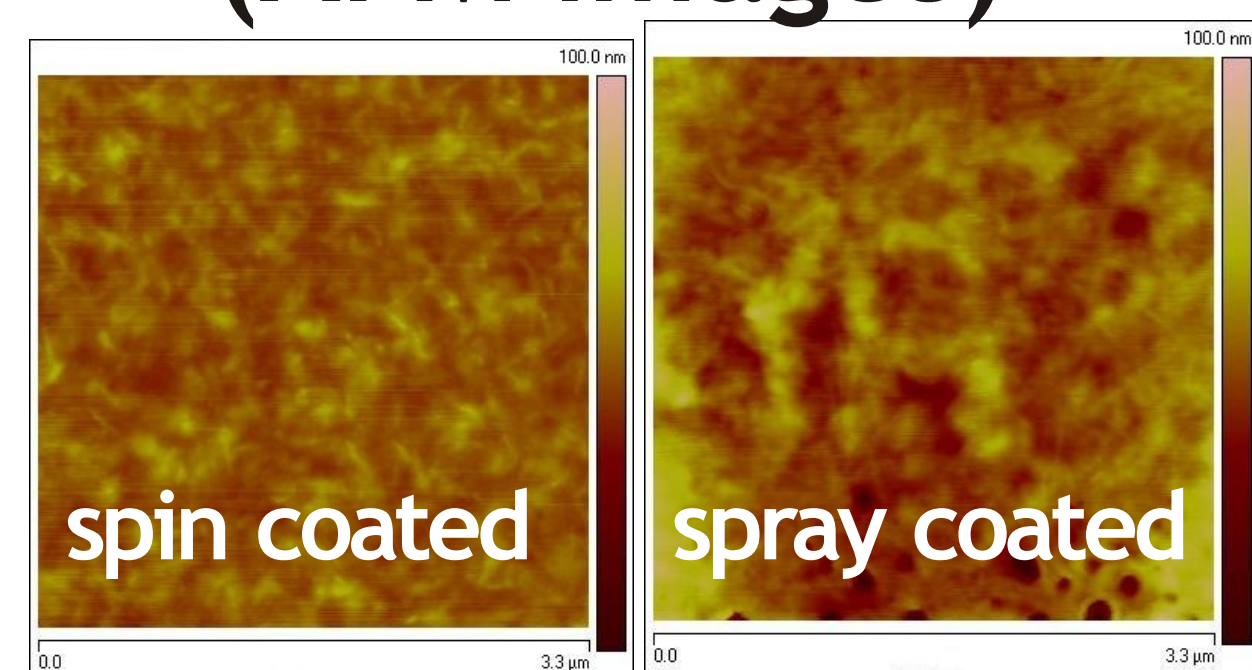
The aim of the present study is to test the performance of novel organic FETs and switches consisting of plotter-printed electrodes and spray-deposited semiconductor. Poly(3-hexylthiophene) (P3HT) and Si/SiO₂ substrates were used as organic semiconductor and gate electrode with insulator, respectively. The source-drain electrodes of FETs were printed using a PEDOT:PSS aqueous solution, with a piezoelectric-assisted microplotter (SONO PLOT).

The characteristics of FETs with printed electrodes were analyzed and compared with those of FETs with photolithographically deposited gold electrodes. The mobilities of charge carriers in both types of devices were of the same order (10⁻³ cm²/Vs). The threshold voltages in FETs with printed PEDOT:PSS electrodes were significantly lower than those in the devices with gold electrodes (-10 V compared to -25 V), evidencing good prospects of the new technique for practical application.

Surface morphology of source and drain electrodes



Surface morphology of P3HT on SiO2 (AFM images)



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Photoswitching of an n-Type Organic Field Effect Transistor by a Reversible Photochromic Reaction in the Dielectric Film

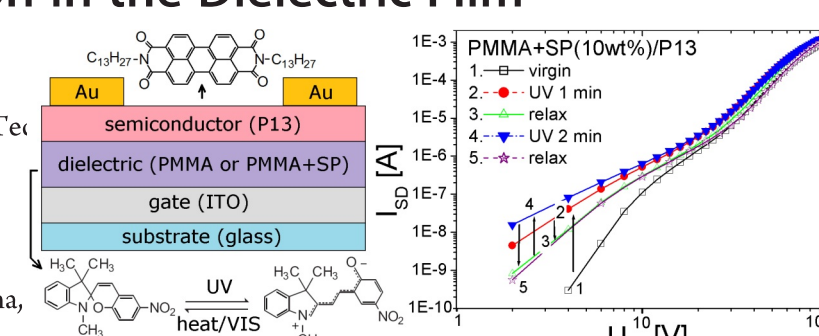
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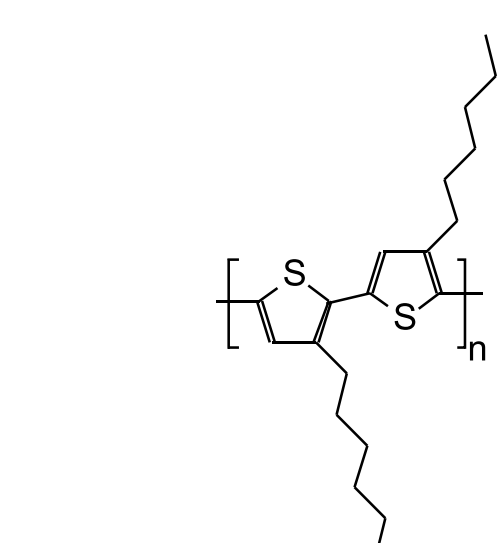
dx.doi.org/10.1021/jp108982x | J. Phys. Chem. C 2011, 115, 3106-3114



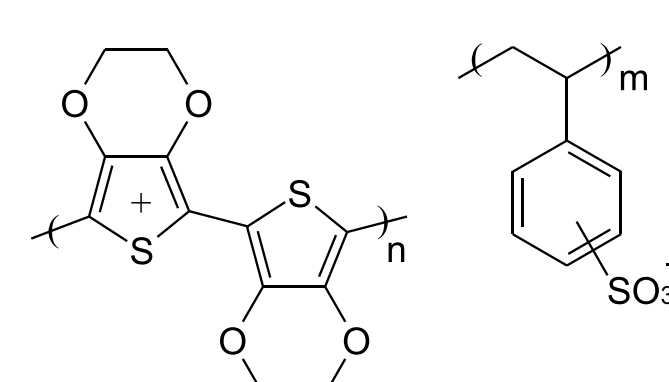
REFERENCES

- [1] H. Klauk (Ed.), Organic Electronics, Wiley-VCH Weinheim, 2006.
- [2] H. Cheun, P. P. Rugheimer, B.J. Larson, P. Gopalan, M.G. Lagally, M.J. Winokur, J. Appl. Phys. 100 (2006) 073510.

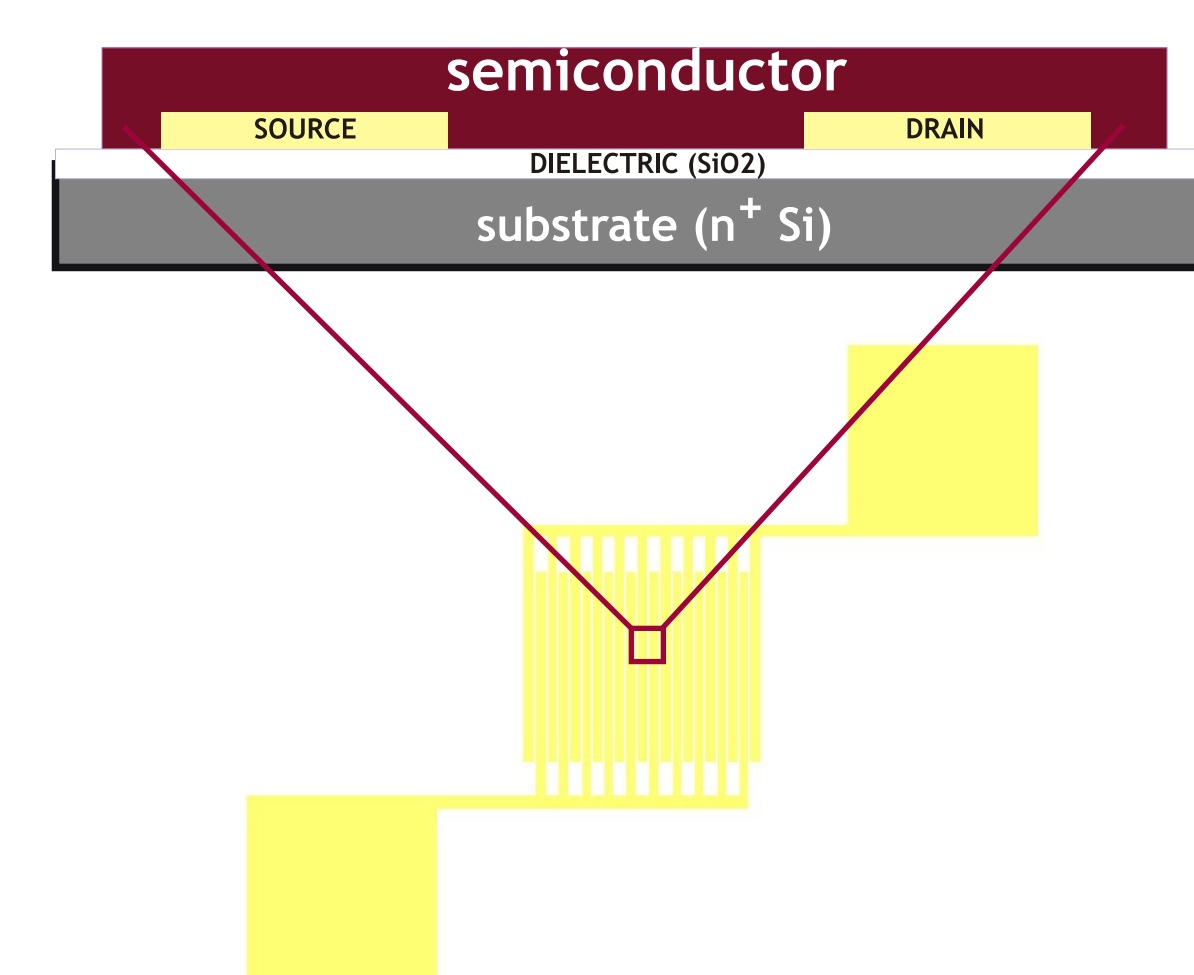
MATERIALS and SUBSTRATES



Semiconductor: poly(3-hexylthiophene) (P3HT) from Ossila



Source and drain electrodes: mixture of poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) from Aldrich



Silicon(n+)/SiO₂ wafers (Fraunhofer-Institut Photonische Microsysteme, Dresden) were used as substrates for PEDOT:PSS printing

The FET substrates with gold source and drain electrodes were also purchased from Fraunhofer-Institut Photonische Microsysteme

FET current-voltage characteristics

SATURATION REGIME [$I_{SD}(U_{SD}) = \text{const}$]:

I_{SD} and U_{SD} stand for source-drain current and voltage respectively;

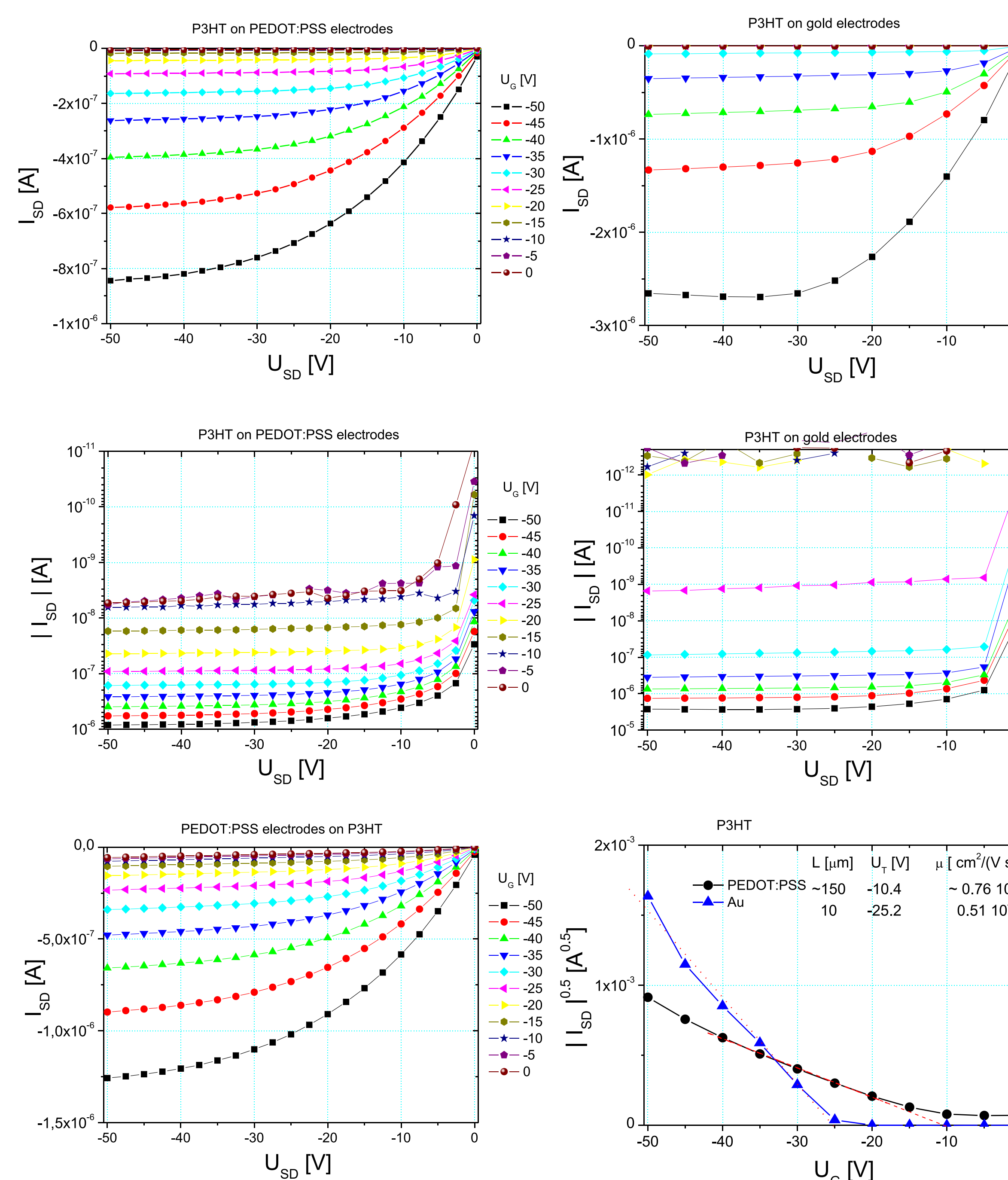
μ is mobility of charge carriers;

W and L stand for width and length of the channel, respectively;

C is surface capacitance of the insulator between gate and source-drain electrodes.

$$I_{SD} = \mu \frac{WC}{2L} (U_G - U_T)^2$$

$$\mu = \frac{2L}{WC} \left(\frac{I_{SD}^{0.5}}{U_G - U_T} \right)^2$$



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