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Fully Printed Stretchable Thin-Film Transistors and Integrated Logic Circuits

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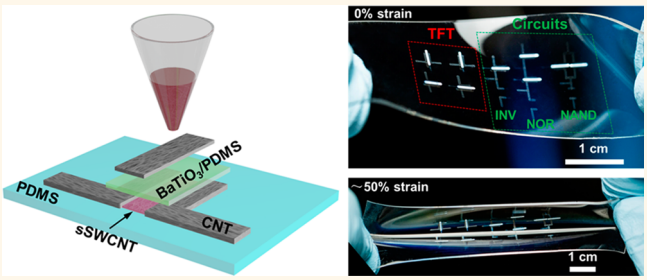
Supporting Information

ABSTRACT: This paper reports intrinsically stretchable thin-film transistors (TFTs) and integrated logic circuits directly printed on elastomeric polydimethylsiloxane (PDMS) substrates. The printed devices utilize carbon nanotubes and a type of hybrid gate dielectric comprising PDMS and barium titanate ($BaTiO_3$) nanoparticles. The $BaTiO_3$/PDMS composite simultaneously provides high dielectric constant, superior stretchability, low leakage, as well as good printability and compatibility with the elastomeric substrate. Both TFTs and logic circuits can be stretched beyond 50% strain along either channel length or channel width directions for thousands of cycles while showing no significant degradation in electrical performance. This work may offer an entry into more sophisticated stretchable electronic systems with monolithically integrated sensors, actuators, and displays, fabricated by scalable and low-cost methods for real life applications.



KEYWORDS: *stretchable electronics, printed electronics, thin-film transistors, integrated circuits*

Stretchable electronic systems built on soft substrates offer more conformal surface coverage and better durability than flexible electronics and have generated significant research interest recently for potential applications in wearable/implantable health monitoring and diagnostic devices,[1−3] electronic skin for prosthesis or soft robotics,[4,5] stretchable displays,[6,7] and more. Nevertheless, the required large area and low-cost fabrication of high-performance intrinsically stretchable electronic devices have remained extremely difficult. There are three key technical challenges faced by large-area stretchable electronics: (1) high-performance and robust stretchable electronic material platforms; (2) scalable and low-cost fabrication processes; and (3) integration of stand-alone stretchable devices into functional systems. Stretchable electronics are generally realized through two approaches, namely, structural stretchability enabled by the use of buckling or serpentine structures in stiff materials or intrinsic stretchability endowed by new elastomeric or composite materials.[8] The first structural engineering approach utilizes high-performance rigid semiconductors (*e.g.*, silicon or III−V materials) and conventional clean-room-based microfabrication processes, which have led to the demonstration of numerous types of sophisticated stretchable electronic systems.[1,9,10] Despite the great success, this first approach may not be suitable for certain large-area applications due to the high manufacturing cost. Moreover, only a fraction of the area is actually occupied by active devices, and the rest of the area is filled with voids and thus wasted. In this regard, intrinsically stretchable materials are of particular interest because they are usually solution processable and even printable and, thus, potentially suitable for large-area and cost-effective manufacturing.[11,12] A number of new materials have been under exploration, among which are silver nanowires,[13] carbon nanotubes,[14−16] graphene,[17] conductive polymers,[18] and organic semiconductors.[19] Intrinsically stretchable thin-film transistors (TFTs) have been demonstrated recently by a variety of approaches based on the above materials.[20−26] However, printing has never been used as the fabrication process, and all previous reports were only limited to proof-of-concept level demonstrations of individual transistors.

RESULTS AND DISCUSSION

In this work, we take one significant step forward by demonstrating fully printed stretchable integrated circuits on PDMS substrates. Unsorted carbon nanotubes (CNTs) and high-purity semiconducting single-walled carbon nanotubes (sSWCNTs) are used as the source/drain/gate electrodes and channel semiconductor, respectively. As shown in the schematic (Figure 1a) and optical micrograph (Figure 1b), our stretchable

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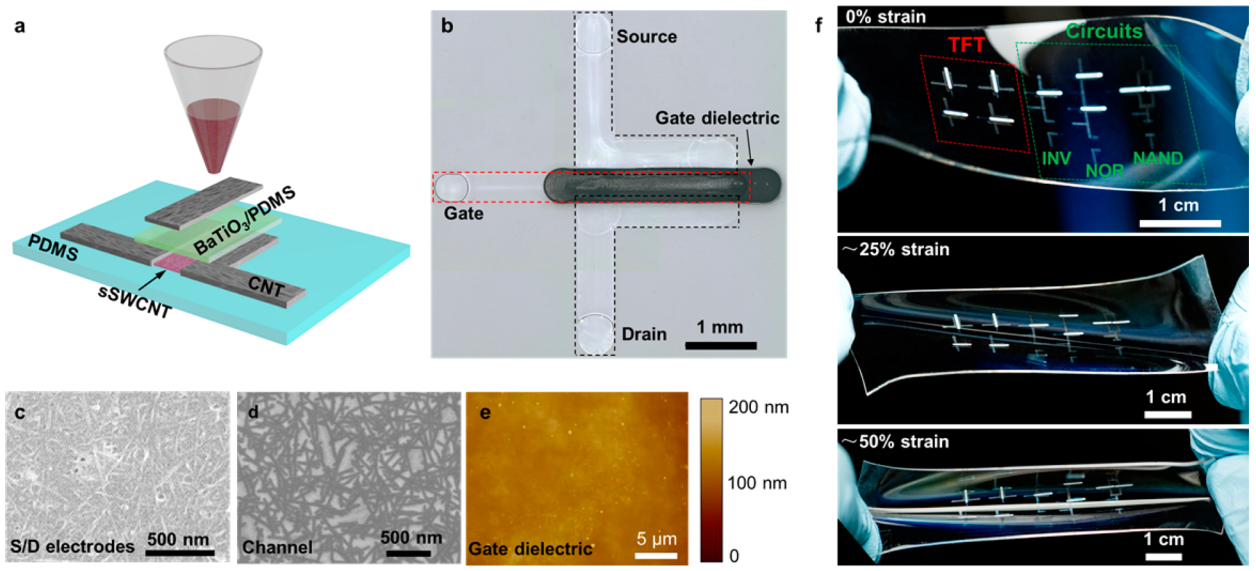

Figure 1. Fully printed and intrinsically stretchable carbon nanotube thin-film transistors (TFTs) and integrated logic circuits. (a) Schematic illustrating the structure of a printed stretchable TFT. Unsorted carbon nanotubes, high-purity semiconducting single-walled carbon nanotubes (sSWCNT), and $BaTiO_3$/PDMS composite are used as the source/drain/gate electrodes, channel semiconductor, and gate dielectric, respectively. (b) Optical micrograph of a TFT printed on a PDMS substrate. (c–e) Scanning electron micrograph of the carbon nanotube network in the source/drain electrodes (c) and channel (d) and atomic force micrograph of the $BaTiO_3$/PDMS gate dielectric (e). (f) Optical photograph of a representative sample consisting of four TFTs, a resistive load inverter, and a resistive load two-input NOR gate and NAND gate, at tensile strains of 0% (top), ~25% (middle), and ~50% (bottom).

TFTs were fabricated using an all-printing process and adopt a top-contact, top-gated device structure (see the Methods and Supporting Information S1 for more details). Compared with silver or gold nanoparticle inks, the most widely used conducting materials in printed electronics, CNT electrodes provide better electrode–semiconductor contacts due to the perfect structural and electronic consistency between carbon nanotubes.[27] In addition, carbon nanotubes are a perfect choice for stretchable electrodes because of their ultrahigh aspect ratio and the formation of highly deformable mesh structures in macroscale assemblies.[14] Parts c and d of Figure 1 reveal the dense unsorted CNT network in the source/drain electrodes and the monolayer sSWCNT network in the TFT channel region. The gate dielectric is a composite consisting of PDMS, the same material as the stretchable substrate, and $BaTiO_3$ nanoparticles, a ceramic material with a relative permittivity of up to ~200. This hybrid dielectric material combines the best of both worlds; *i.e.*, the high permittivity of $BaTiO_3$ and superior stretchability of PDMS, as shown below, deliver excellent electrical performance, mechanical robustness, and compatibility with the substrate. The atomic force micrograph (AFM) of the printed $BaTiO_3$/PDMS is shown in Figure 1e. Figure 1f presents photographs of a representative sample with printed TFTs and integrated logic circuits (inverter, NOR, and NAND gates) in the relaxed state and under tensile strain of ~25% or ~50%.

The unsorted carbon nanotubes used for the electrodes and interconnections are purified with nitric acid and contain 1.0–3.0 atomic percent carboxylic acid,[28] and thus, they can be well dispersed in pure water without the assistance of any surfactant. Experiments show that back-gated TFTs fabricated on Si/SiO_2 substrates with printed CNT ink as the source/drain electrodes exhibit comparably high performance as those with thermally evaporated metal electrodes (Figure S2). Printing aqueous inks directly onto PDMS is, however, very challenging because the surface of PDMS is extremely hydrophobic. Although it is possible to render the PDMS surface hydrophilic by O_2 plasma or UV ozone treatments, it recovers its hydrophobicity very quickly, especially under elevated temperatures that are sometimes required for printing processes. By adding a small amount (0.1% wt) of Triton X-100 to tune the surface tension of the CNT solution, we were able to print carbon nanotubes on PDMS directly with very well-defined and uniform features (Figures S3 and S4). Since the CNT solution has a quite low concentration (<0.5 mg/mL), multiple printing runs are required to obtain a conductive feature. Figure 2a presents the resistance of the printed CNT features after various numbers of printing runs. The resistance drops dramatically during the first ~20 runs and reaches several kΩ after ~40 runs, which is sufficiently low to work as the source/drain electrodes for CNT TFTs (channel resistance is greater than hundreds of kΩ). Extensive studies have shown that, due to the one-dimensional attributes of CNTs and the mesh structure of their macroscale assemblies, CNT thin films exhibit excellent stretchability.[14] Additionally, the increase in resistance under tensile strain can be further alleviated by a polymeric encapsulation layer.[29] Comparing the pristine CNT features printed on PDMS with those encapsulated by an additional PDMS layer, one can clearly see that the encapsulated CNT film exhibits better stretchability, with a change in resistance of ~200% under 60% tensile strain (Figure 2b). The critical role of PDMS encapsulant in improving the stretchability of the CNT film can be attributed to the greatly mitigated stress concentration in CNT networks by the surrounding cross-linked PDMS molecules, which prevents the occurrence of macroscale cracks that are responsible for a more pronounced increase in resistance of the unencapsulated features (Figure S5). After hundreds of stretching cycles with a maximum strain of 60%, the resistance of an encapsulated CNT features settles at around 5 times of its original value (Figure 2c).

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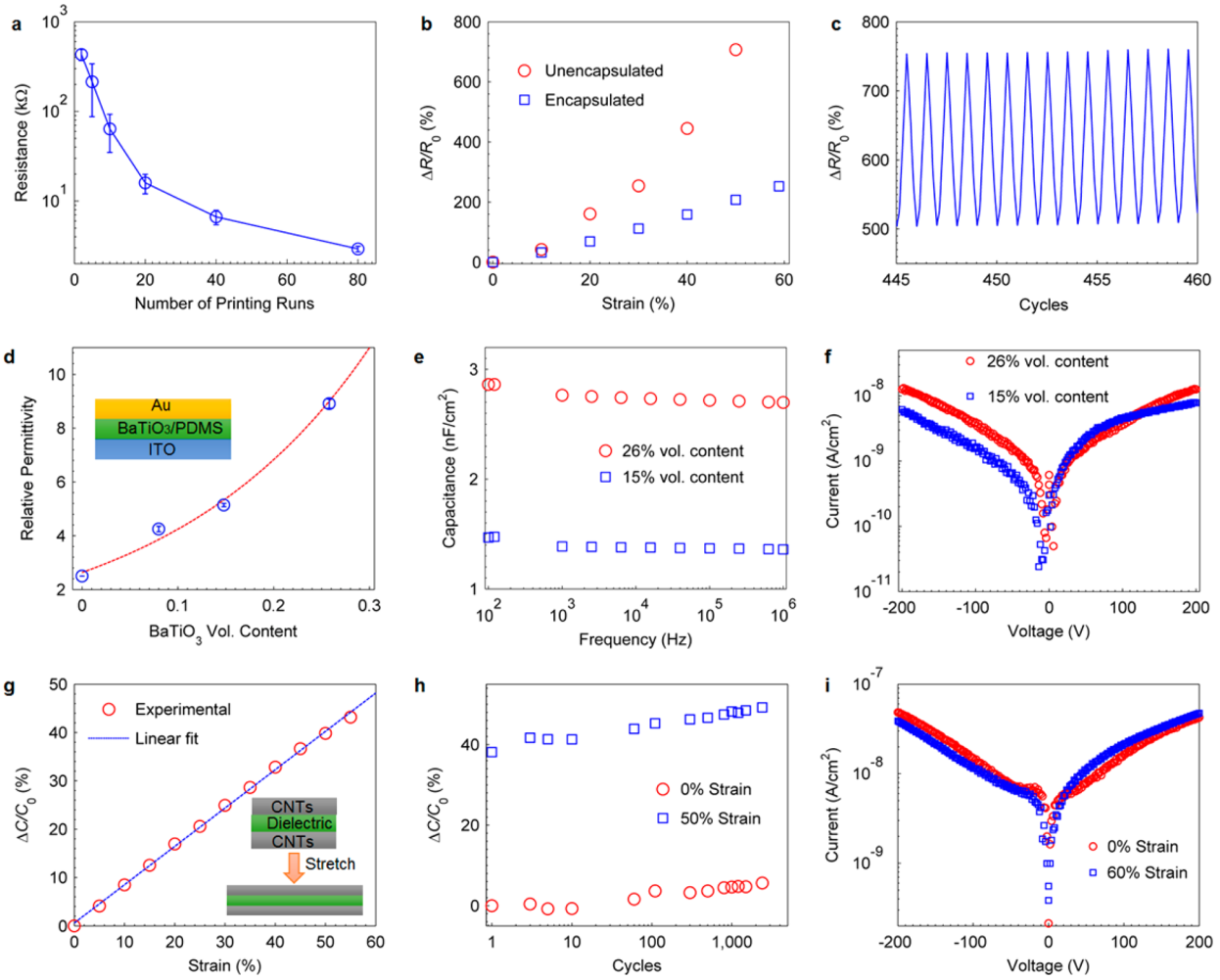

Figure 2. Characteristics of the printed CNT electrodes and $BaTiO_3$/PDMS gate dielectric. (a) Resistance of CNT features (length ~6 mm, width ~0.5 mm) printed on PDMS as a function of the number of printing runs. The error bars are standard deviations obtained from more than five samples. (b) Relative change in resistance ($\Delta R/R_0$) as functions of tensile strain for CNT features with (blue squares) and without (red circles) PDMS encapsulation layer. (c) $\Delta R/R_0$ of a printed CNT feature (with PDMS encapsulation) when the sample is being repeatedly stretched between 0% and 60% strain. (d) Relative permittivity of the composite gate dielectric as a function of the volume content of $BaTiO_3$ nanoparticles measured from parallel plate capacitors fabricated on glass substrate. The error bars are standard deviations obtained from more than five samples. Inset: cross-sectional schematic of the parallel plate capacitor. (e) Capacitance measured at various frequencies for the composite gate dielectrics with $BaTiO_3$ volume content of 15% (blue squares) and 26% (red circles), respectively. (f) Leakage current density of the composite gate dielectric with a thickness of around 2 μm. (g) Relative change in capacitance ($\Delta C/C_0$) as a function of tensile strain measured from a parallel plate capacitor printed on PDMS. Inset: cross-sectional schematics of the capacitor at relaxed state and stretched state. (h) $\Delta C/C_0$ at 0% (red circles) and 50% (blue squares) strains measured during repeated stretching tests for more than 2, 000 cycles. (i) Leakage current density of the composite gate dielectric measured at 0% (red circles) and 60% (blue squares) strains.

One of the greatest challenges in realizing intrinsically stretchable TFTs is the high-performance stretchable gate dielectric material that can simultaneously offer high gating strength, good mechanical robustness, and solution processability.[14,20] Conventional inorganic gate dielectrics like SiO_2 and Al_2O_3 are rigid and brittle and, thus, not suitable for stretchable devices unless engineered to a wrinkled configuration by sophisticated approaches.[20] In addition, they usually require vacuum-based deposition processes (evaporation or atomic layer deposition), which are costly and not suitable for low-cost applications or green manufacturing. A number of alternative material platforms, like polymeric dielectrics,[22,26] ion gels,[21,24,25] and hybrid dielectrics,[30] have been proposed. Solution-processed polymeric dielectrics have been widely used for both flexible and stretchable TFTs, but most of them exhibit rather low dielectric constants and gating strength, which leads to high operating gate voltages. Ionic gels (block copolymer networks swollen by ionic liquids) have also attracted extensive research interest as stretchable gate dielectric materials due to their gigantic capacitance and superior stretchability.[31] The practical applications of ion gels are, however, greatly hampered by their instability in ambient conditions, difficulties in suppressing gate leakage current, and possible electrochemical reactions at the dielectric/conductor or dielectric/semiconductor interface. In contrast, hybrid dielectrics consisting of inorganic dielectric nanofillers dispersed in a polymer matrix show the best overall performance by combining the high permittivity of inorganic dielectrics with the solution processability and mechanical robustness of polymers. A large variety of inorganic high-k dielectric and polymer composites have been explored.[30] For instance, several groups have demonstrated that the $BaTiO_3$/PMMA composites

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show excellent performance as the gate dielectric for printed flexible CNT TFTs.[32−34] Despite the progress, almost all studies focus on hybrid dielectrics that are only flexible and cannot survive large tensile deformations. Here in this work, we have developed a highly stretchable hybrid gate dielectric material by blending cubic phase $BaTiO_3$ nanoparticles (particle size ∼50 nm) and PDMS (see the details in the Methods and Supporting Information). 4-Methyl-2-pentanone was chosen as the solvent because it not only dissolves PDMS very well but also has a vapor pressure and surface tension suitable for printing (Table S1).

Systematic electrical characterizations (Figure 2d−i) reveal that the $BaTiO_3$/PDMS hybrid dielectric exhibit superior performance in almost all aspects, including dielectric constant, high frequency characteristics, leakage current, and stretchability. $BaTiO_3$/PDMS dispersions were prepared with $BaTiO_3$ volume content of up to ∼26% (see Supporting Information S7 for volume content calculation) and can be coated on various substrates by spin-coating or direct printing. As shown in Figure 2d, the relative permittivity increases dramatically and reaches ∼9 at a $BaTiO_3$ volume content of ∼26%. Inks with higher $BaTiO_3$ contents are very difficult to be dispersed evenly. The relative permittivity *versus* $BaTiO_3$ volume content can be fitted very well by the well-known Lichtenecker's equation that is widely used to describe composite dielectric systems with spherical fillers[35]

$$\ln(\varepsilon_{cr}) = f \ln(\varepsilon_{fr}) + (1 - f) \ln(\varepsilon_{mr}) \quad (1)$$

where ε_{cr}, ε_{fr}, and ε_{mr} are the relative permittivities of the composite, nanofiller, and polymer matrix, respectively, and f is the volume content of the nanofiller. The fitting parameters obtained here, $\varepsilon_{fr} \sim 307.9$, $\varepsilon_{mr} \sim 2.6$, are close to the relative permittivity of cubic phase $BaTiO_3$ and PDMS, respectively. The results here imply that hybridization is an effective approach to greatly enhance the dielectric constant of polymers while maintaining their desirable mechanical property and solution processability.

The gigantic capacitance in ionic gel dielectric originates from the establishment of electrical double layers, which relies on the migration of mobile ions in an electric field and is very slow.[31] In contrast, our $BaTiO_3$/PDMS composite only undergoes dielectric polarization when placed in an electric field and thus exhibits significantly better high frequency performance. Figure 2e shows the capacitance-frequency characteristics of parallel plate capacitors made with the $BaTiO_3$/PDMS dielectrics with ∼15% or ∼26% $BaTiO_3$ by volume. As expected, the capacitance is virtually independent of frequency in the range of 100 Hz-1 MHz. We also characterized the leakage current density of our $BaTiO_3$/PDMS hybrid dielectric using the parallel plate capacitor with a dielectric layer thickness of ∼2 μm. As shown in Figure 2f, regardless of the volume content of $BaTiO_3$, the leakage current density remains below 10 nA/cm^2 under a voltage of 200 V (electric field of ∼1 MV/cm). For a TFT with a channel footprint of 2000 × 200 μm, such leakage current density corresponds to a gate leakage current of ∼40 pA. The extremely low leakage current implies that the $BaTiO_3$ nanoparticles have very good compatibility with the PDMS matrix and the dielectric layer is free of pinholes.

As discussed above, one of the most intriguing merits of hybrid dielectrics is that they inherit the mechanical properties of polymers,[30] which is manifested by the stretching tests on the parallel plate capacitors fabricated on PDMS substrates. Unsorted carbon nanotubes were printed as the top and bottom electrodes of the capacitors (see Supporting Information S1 for fabrication details). The inset of Figure 2g illustrates the device structure and its geometric variations under tensile strains. When the capacitor is subjected to tensile strain, it will extend along the stretching direction (l direction) and shrink along the other two perpendicular directions (w and t directions) due to the Poisson effect. The capacitance at zero strain and under tensile stretch can be written as $C_0 = \varepsilon_{zero}\frac{l_0 w_0}{t_0}$ and $C = \varepsilon\frac{(\lambda_1 l_0)(\lambda_2 w_0)}{\lambda_3 t_0}$, respectively, where ε_{zero} represents the permittivity of the dielectric at zero strain and ε is the permittivity under strain. Here, the extending ratio along the stretching direction, λ_1, equals to $1 + \epsilon$, where ϵ is the tensile strain. For an isotropic material like PDMS, the compression ratios along the other two directions, λ_2 and λ_3 should have the same value. Given that the permittivity is independent of tensile strains, the capacitance under tensile strain can be written as $C = (1 + \epsilon)C_0$, so that the relative change in capacitance is $\Delta C/C_0 = \epsilon$. In other words, the relative change in capacitance is linear to the tensile strain with a slope of 1.[29] The experimental data of $\Delta C/C_0$ *versus* tensile strains for a parallel plate capacitor using $BaTiO_3$/PDMS dielectric (Figure 2g) can be fitted very well by a linear function with a slope of ∼0.8. The deviation from the theoretical slope of 1 could be explained by the possible anisotropy induced by the presence of $BaTiO_3$ nanoparticles in PDMS. In addition, the permittivity of the composites might be slightly dependent on tensile strains, which deserves further study. The increase in capacitance upon stretching leads to a stronger gating strength and thus, as will be discussed below, benefits the performance of the stretchable CNT TFTs.

Cyclic stretching tests were performed to study the durability of the $BaTiO_3$/PDMS composite dielectric. Figure 2h presents the $\Delta C/C_0$ (C_0 represents the pristine capacitance) of a device repeatedly stretched between 0% and 50% strains for 2000 cycles. The $\Delta C/C_0$ at 0% and 50% strain both show very slight increasing trend with roughly the same rate over the entire stretching test, which is different from the capacitors with pure silicone dielectric.[29] The reason for this synchronous shift is unclear at this moment and requires more detailed studies. One possible explanation is the reassembly of $BaTiO_3$ nanoparticles by migration inside the PDMS molecule network under the stimulation of cyclically changing stress fields.[36] We also monitored the change in leakage current during the stretching tests as shown in Figure 2i. It is impressive that the leakage current showed virtually no change when the device is stretched to 60% strain, implying the superior robustness of the $BaTiO_3$/PDMS dielectric and no formation of pinhole or crack during the stretching process. An additional advantage of the $BaTiO_3$/PDMS hybrid gate dielectric is its excellent compatibility with the PDMS substrate, as manifested by the fact that no sliding between the dielectric and PDMS substrate was observed at a tensile strain up to 100% (Figure S6), which is significantly better than ionic gels.[25] Lastly, to confirm that the $BaTiO_3$/PDMS works well as gate dielectric for CNT TFTs, top gated TFTs with evaporated gold source/drain electrodes and printed $BaTiO_3$/PDMS dielectric and CNT gate electrode were assembled on silicon substrates. Details can be found in Supporting Information S9 and Figure S7. The results indicate that the printed $BaTiO_3$/PDMS hybrid dielectric outperforms 300 nm thick high-quality thermally grown SiO_2 dielectric by

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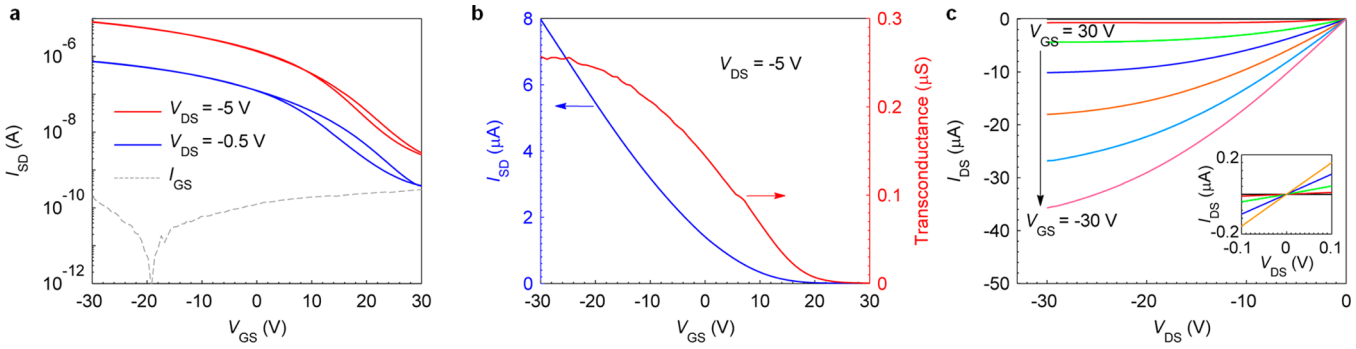

Figure 3. Representative electrical characteristics of the fully printed stretchable TFTs on PDMS. (a) Semilogarithmic scale plot showing the forward and backward sweep transfer characteristics ($I_{SD} - V_{GS}$) of a TFT measured at V_{DS} of −5 V (red) and −0.5 V (blue) and the gate leakage current curve ($I_{SG} - V_{GS}$) measured at V_{DS} of −0.5 V (gray dashed line). (b) I_{SD} (blue) and transconductance (red) as functions of V_{GS} plotted in linear scale for the same device in panel (a). (c) Output characteristics of the same TFT with V_{GS} varying from 30 V to −30 V. Inset shows the $I_{DS} - V_{DS}$ curves under low drain bias indicating negligible Schottky barriers at the semiconductor and S/D electrode interfaces.

providing TFTs with better field-effect mobility and on/off current ratios.

Based on the stretchable CNT electrodes and $BaTiO_3$/PDMS hybrid gate dielectric developed above, stretchable TFTs were successfully fabricated on PDMS substrates by an all-printing process. Such printed TFTs typically have channel lengths (L) and channel widths (W) of ∼150−200 μm and ∼2500 μm, respectively. Figure 3 presents the representative transfer ($I_{SD} - V_{GS}$) and output ($I_{SD} - V_{DS}$) characteristics of the stretchable TFTs. The transfer curves presented in Figure 3a show good overlap between the forward and backward sweeps, indicating that hysteresis is nearly absent in our devices. In addition, according to the gray dashed line in Figure 3a, the gate leakage current remains at a reasonably low level (∼100 pA for V_{GS} = 30 V), which is in good agreement with the values measured from parallel-plate capacitors in Figure 2i. Linear scale transfer curve and tranconductance (g_m) *versus* V_{GS} of the same device are shown in Figure 3b. The output characteristics presented in Figure 3c show unambiguous saturation behavior at high drain voltages that is typical for field-effect transistors and excellent linearity at low bias regime (Figure 3c inset), indicating negligible Schottky barrier at the interfaces between the channel semiconductor and source/drain electrodes. Most of our devices exhibit field effect mobility around 4 $cm^2V^{-1}s^{-1}$ and on/off ratio greater than 500 with maximum values of 7 $cm^2\ V^{-1}\ s^{-1}$ and 3000, respectively, which is respectable for the all-printing process.

Next, we investigated the electromechanical properties of the CNT TFTs printed on PDMS by performing systematic stretching tests along both channel length and channel width directions. The optical micrographs in Figure 4a and b reveal the geometric variations of two devices being stretched along L and W directions, respectively. When the device is stretched along L direction, the channel length elongates and channel width decreases (due to Poisson effect), while the opposite changes (W increases, L decreases) will take place under tensile strain along W direction. The geometric variations are also reflected by the dimensional changes of the source/drain and gate electrodes, whose boundaries are marked by dashed lines. The geometric changes in the channel, as shown below, will have an effect on the TFT characteristics. Parts c and f of Figure 4 present the evolution of transfer curves at V_{DS} of −0.5 V while the device is stretched up to 50% strain along the channel length and channel width directions, respectively. The on-state current drops by about one-half of its pristine value at 50% tensile strain along the L direction, while a very small decrease is observed under the same strain along the W direction. Meanwhile, the off-state current is drastically suppressed for both cases. The effects of tensile strain on the TFT drain current (I_{DS}) can be interpreted by three primary factors, namely the geometric change of the channel, the initiation and propagation of cracks in the sSWCNT network, and the enhancement in gating strength due to thinner gate dielectric. First, assuming the sSWCNT network and gating strength do not change, I_{DS} is proportional to the ratio of channel width to channel length (W/L), so I_{DS} would decrease when stretched along L direction and increase when stretched along W direction. Second, it is well-known that the surface of PDMS will be covered by a very thin layer of silica after O_2 plasma treatment, which is a crucial step for our printing recipe. The silica skin is extremely brittle and, hence, forms ubiquitous cracks when the PDMS substrate is subjected to tensile strain. Consequently, many cracks appear in the otherwise continuous sSWCNT network following the deformation of the silica skin.[29] As a result, many percolating pathways are cut off, leading to a reduction in I_{DS}. Considering both the influence of geometric change of the channel and structural change of the sSWCNT network, one can easily understand the distinct behaviors of on-state current when stretched along different directions. It is worth mentioning that the formation of cracks in the channel has a larger influence on the metallic percolation pathways than on the semiconducting ones because the sSWCNT ink used here contains only 2% metallic nanotubes, which is beneficial for the improvement of on/off current ratio under tensile strain. Finally, the $BaTiO_3$/PDMS dielectric layer will also become thinner under tensile strain (see Figure 2g), which contributes to a stronger gating strength and consequently further suppression of the off-state current. The upper panels of Figure 4e,h present the device field-effect mobility (left axis) and on/off current ratio (right axis) as functions of tensile strains along the L direction and W direction, respectively. Device mobility (μ) is extracted using the equation in linear region $\mu = g_mL/(WV_{DS}C_{ox})$, where g_m and C_{ox} are transconductance and gate capacitance, respectively. Gate capacitance is determined by direct capacitance−voltage (C−V) measurements on the TFTs and considering the geometric changes of the channel. Regardless of stretching direction, mobility decreases by about 1/3 of its original value under 50% strain, reflecting the microscopic structural changes in the sSWCNT networks discussed above. On the other hand,

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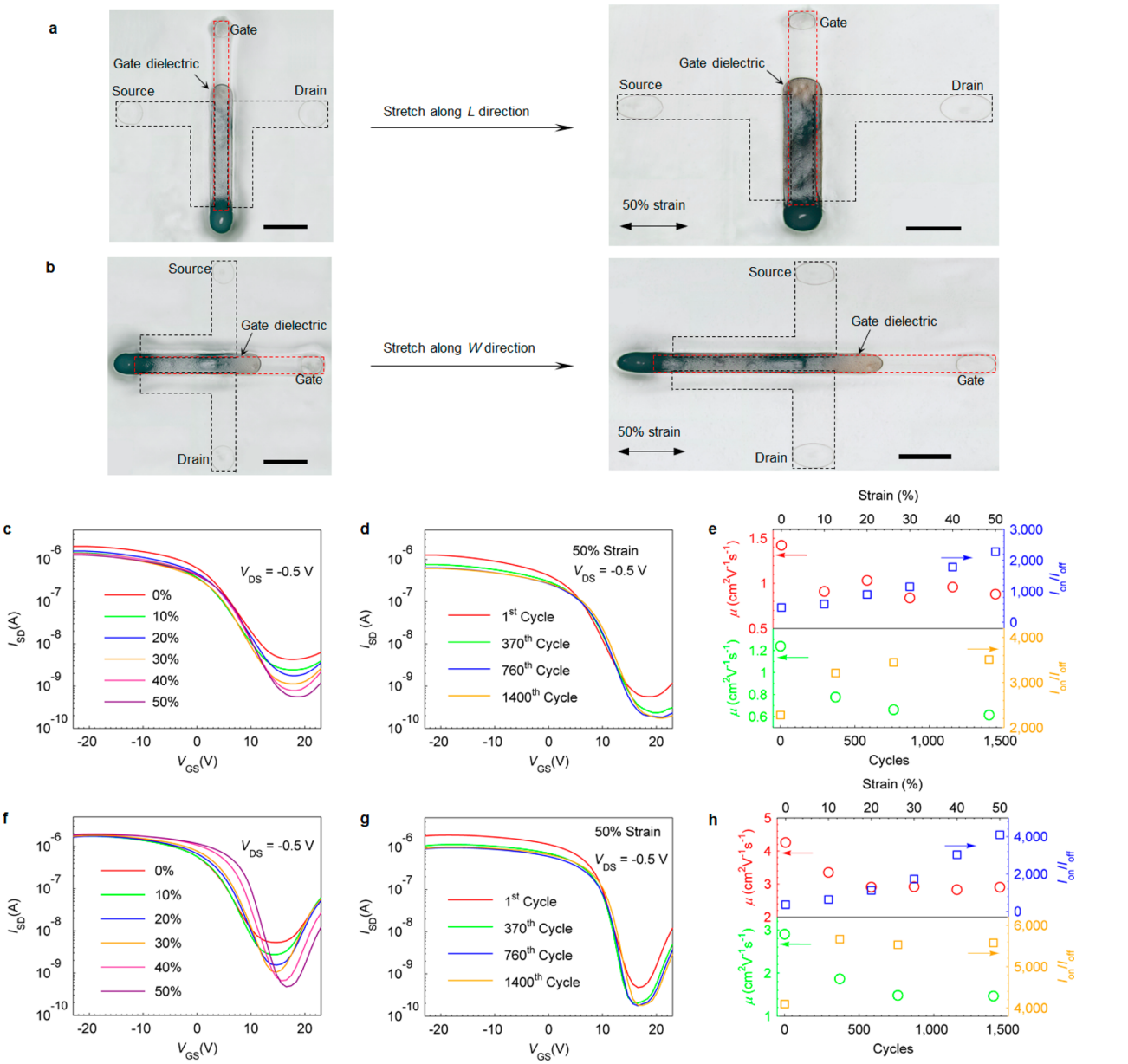

Figure 4. Stretching tests of the printed CNT TFT on PDMS substrate. (a, b) Optical micrographs showing two devices stretched along channel length (a) and channel width (b) directions, respectively. Scale bars represent 1 mm. (c, f) Transfer characteristics at V_{DS} of −0.5 V, while the devices are stretched to various strain levels along the channel length (c) and channel width (f) directions, respectively. (d, g) Transfer characteristics at V_{DS} of −0.5 V, while the device is stretched to 50% strain for the 1st time (red), the 370th time (green), the 760th time (blue), and the 1400th time (orange) along channel length (d) and channel width (g) directions, respectively. (e, h) Field-effect mobility (left axes) and on/off current ratio (right axes) as functions of tensile strain (upper panel, in the 1st cycle) and stretching cycles (lower panel, at 50% strain) along channel length (e) and channel width (h) directions, respectively.

the on/off ratio increases by almost 1 order of magnitude due to the significantly suppressed off-state current. Figure S8 presents the output characteristics of another device being stretched along the channel length direction. The current level drops to about 1/3 of the pristine value after being stretched to 60% strain for the first time and remains nearly unchanged afterward when the tensile strain is released. Regardless of the tensile strain, the device maintains very standard MOSFET characteristics with clear saturation regions in the output curves. The maximum tensile strain that our device can withstand exceeds 50% and is actually limited only by the rupture of PDMS substrates. We have tested more devices, and some of them can be stretched to 100% strain with electromechanical behaviors similar to those described above (Figure S9).

The stretchable CNT TFTs were then subjected to long-term cyclic stretching with a maximum strain of 50%. The transfer characteristics at 50% strain after different numbers of cycles are shown in Figure 4d (stretching along L direction) and Figure 4g (stretching along W direction). The device field-effect mobility (left axis) and on/off current ratio (right axis) at 50% strain are plotted as functions of stretching cycles in the lower panels of Figure 4e and h for stretching along the L and W directions, respectively. Upon repeated stretching, the on-state current, off-state current, and mobility drop further while the on/off current ratio continues to increase, which could be

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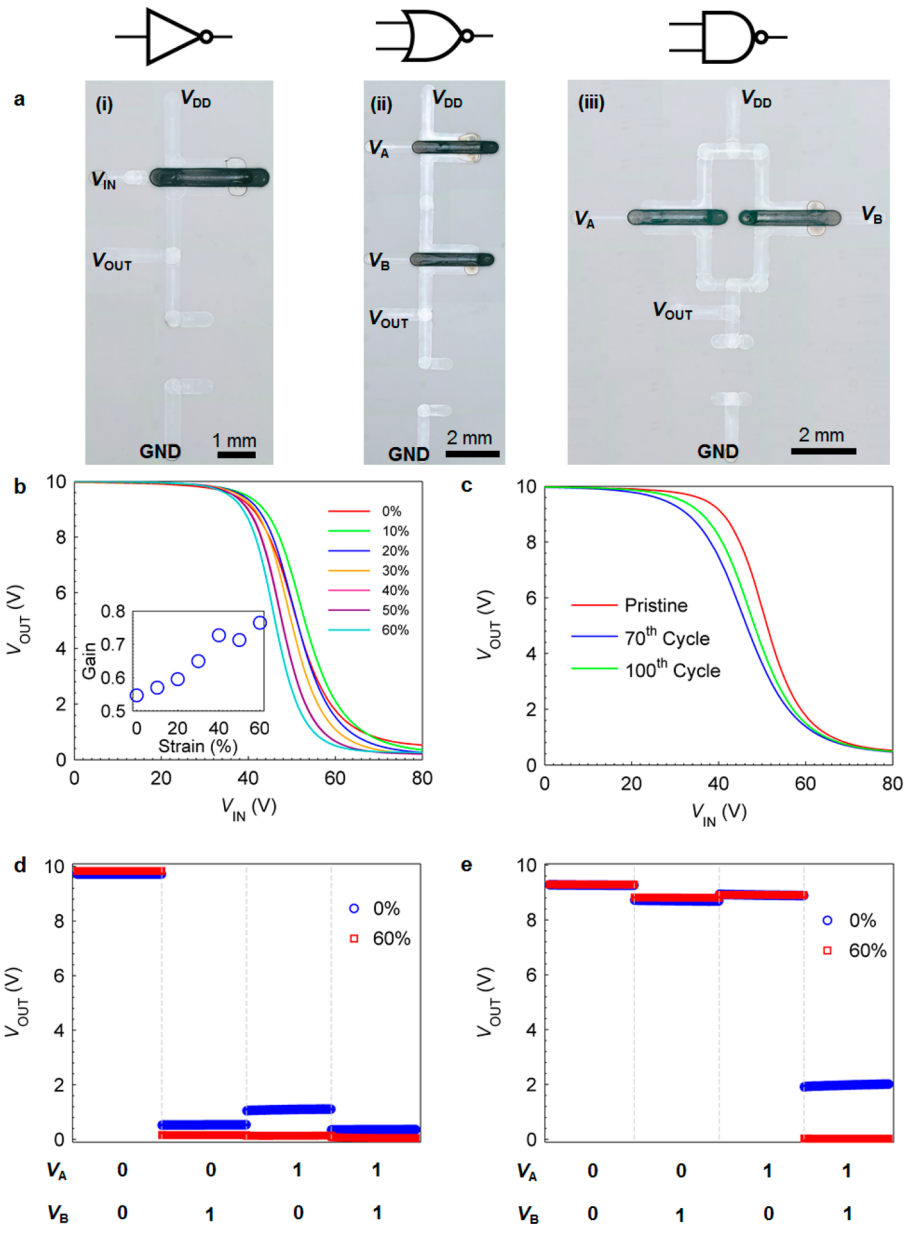

Figure 5. Fully printed stretchable integrated logic circuits on PDMS. (a) Optical micrographs of a printed resistive load inverter (i), a resistive load two-input NOR gate (ii), and a two-input NAND gate (iii). (b) Inverter voltage transfer characteristics (VTCs) measured with a V_{DD} of 10 V, while the device is stretched to various strain levels along the channel length direction of the driving TFT. Inset shows the inverter gain as a function of tensile strain. (c) Inverter VTCs measured at a V_{DD} of 10 V while the device is at pristine state (0% strain, red) and at 0% strain after 70 (blue) and 100 (green) stretching cycles with a maximum strain of 50% along the channel length direction of the driving TFT. (d, e) Output characteristics of the NOR gate (d) and NAND gate (e) measured at a V_{DD} of 10 V while the device is at pristine state (0% strain, blue circles) and stretched to 60% strain (red squares) along the channel length direction of the driving TFTs. For both NOR gate and NAND gate, input voltages of 80 and 0 V are treated as logic "1" and "0", respectively.

attributed to further expansion of the cracks and probable initiation of new cracks in the sSWCNT networks. All device performance metrics start to stabilize after hundreds of stretching cycles. Figure S10 presents the transfer curves measured at V_{DS} of −0.5 V under 0% and 50% strains at the 1400th stretching cycle for the same devices. Overall, the difference between the transfer curves at 0% and 50% strains is practically negligible for both devices, indicating the TFTs are stabilized and show almost strain-independent electrical performance after more than 1000 stretching cycles. The above results of stretching tests reveal that our printed CNT TFTs exhibit excellent mechanical robustness and can maintain very stable electrical performance under harsh conditions often encountered in real life wearable electronics applications.

We have also successfully demonstrated fully printed stretchable integrated logic circuits on PDMS, including inverter, NOR and NAND gates. Figure 5a shows the optical micrographs of a resistive load p-type inverter (left), a resistive load two-input NOR gate (middle) and a two-input NAND gate (right). We followed similar procedures as those reported in our previous work to fabricate the logic gates (details can be found in the Methods and Supporting Information).[32] In brief, after fabricating the driving TFT, unsorted CNTs were printed in the load resistor layer by layer until an optimal performance

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was achieved. Systematic electrical and electromechanical characterizations were conducted on the stretchable logic circuits. Figure 5b presents the inverter voltage-transfer characteristics (VTCs) with a V_{DD} of 10 V under various strains along the channel length direction of the driving TFT. The inverter exhibits more pronounced rail-to-rail output voltage swing as the tensile strain is increased to 60%, owing to the improved on/off ratio of driving TFT. In addition, repeated stretching tests indicate that the stretchable inverter exhibits very stable performance, as shown in Figure 5c.

The output voltage of a resistive load inverter is determined by the voltage division between the channel resistance ($R_{channel}$) of the driving TFT and the load resistance (R_{load}) and can be expressed as

$$V_{OUT} = V_{DD}R_{load}/(R_{channel} + R_{load}) \quad (2)$$

When the TFT is turned on (low V_{IN} for a p-type TFT), R_{load} is significantly higher than $R_{channel}$; hence, V_{OUT} is approximately equal to V_{DD}; similarly, V_{OUT} is close to 0 when the TFT is turned off (high V_{IN} for a p-type TFT) because $R_{channel}$ is much greater than R_{load}. From eq 2 and considering the evolution of transfer characteristics of the driving TFT discussed in Figure 4, one can easily understand the dependence of inverter VTCs on tensile strains in Figure 5b. A more in-depth study can be found in Figure S11 where we present the dependence of R_{load} and $R_{channel}$ on tensile strains. The off-state channel resistance of the driving TFT increases by more than an order in magnitude when stretched to 60% strain, which is in agreement with the previous results that the TFT off-state current is significantly suppressed under strains (Figure 4c). Using eq 2 and the values of R_{load} and $R_{channel}$ shown in Figure S11a,b, inverter VTCs under various strain levels are calculated (Figure S11c), and the calculated VTCs reproduce the experimental results very well.

Parts d and e of Figure 5 present the output characteristics of the two-input NOR gate and NAND gate measured with a V_{DD} of 10 V, while the circuits are at pristine state (blue circles) and under 60% strain (red squares) along the channel length direction of the driving TFTs. As expected, the NOR and NAND gates both function properly by showing unambiguous output logic "1" and "0" states. Furthermore, the contrast between the two logic states becomes even more pronounced when the circuits are stretched to 60% strain due to the significantly improved on/off current ratio of the driving TFTs. Lastly, the NOR and NAND gates both exhibit very stable electrical performance during repeated stretching tests, as depicted in Figure S12.

CONCLUSION

In summary, by materials and ink formulation development, we have successfully demonstrated intrinsically stretchable thin-film transistors and integrated logic circuits on PDMS using an all-printing process. The devices and circuits can withstand thousands of stretching cycles with tensile strain exceeding 50% along any directions while maintaining respectable and stable electrical performance. This work is significant as it enables a promising approach to realize low-cost and large-area fabrication of stretchable electronics, which may find a wide range of applications in wearable electronics or printed stretchable displays. There is still plenty of room for follow-up research along this direction in further improving the electrical performance, stretchability, and stability of the devices by optimizing the channel semiconductor, gate dielectric layer, and substrate. Although other semiconducting materials like P3HT,[19] layered MoS_2,[23] and SnO_2 nanowires[37] have been exploited as the channel material for stretchable TFTs, carbon nanotubes are still the overall best choice. Using surfactant-free inks with longer nanotubes could potentially diminish the number of intertube junctions and reduce the tube-to-tube junction resistance, which could further improve the device mobility toward that of individual carbon nanotubes.[14] Using longer nanotubes are beneficial to the improvement of stretchability. As for the dielectric materials, higher permittivity is needed to further lower the operating voltage. According to a recent study, composite dielectric with carbon nanotube as fillers at a concentration near the percolating threshold shows gigantic permittivity,[38] which is worth consideration in future studies. As for the substrate, although PDMS is widely used for stretchable electronics, its intrinsic hydrophobicity complicates the printing process and the brittle silica skin formed on its surface after O_2 plasma treatment is prone to form microscopic cracks. Additionally, PDMS also has high O_2 and H_2O permeability, which could compromise the stability of light-emitting devices under ambient conditions. Therefore, alternative elastomeric substrates with easy-handling surface and low gas permeability are needed to further simplify the fabrication process and to improve the device stability. Finally, more research effort should also be devoted to the development of stretchable light-emitting devices, sensors and actuators, as well as circuit design and integration of these elements into more sophisticated circuits and smart systems. There is no doubt that numerous research efforts are still needed to ultimately bring stretchable electronics from academic research to real life commercial products. The results reported in this paper represent an encouraging leap toward this goal.

METHODS

Materials. Polydimethylsiloxane (Sylgard 184, 10:1) slabs with a thickness of ~0.5 mm were prepared as the stretchable substrates. High-purity semiconducting carbon nanotubes (IsoNanotubes-S 98%, 0.01 mg/mL, NanoIntegris) were used as the channel semiconductors. Highly functionalized unsorted carbon nanotubes (P3-SWNT, Carbon Solutions, Inc.) were used for the source, drain, and gate electrodes of the TFTs. Barium titanate nanoparticles ($BaTiO_3$, 99%, 50 nm, cubic), Triton X-100 (laboratory grade) and poly-L-lysine (0.1% w/v in water), and 4-methyl-2-pentanone (99%) were purchased from US Research Nanomaterials, Sigma-Aldrich, and Alfa Aesar, respectively.

Ink Formulations. To prepare the inks for printed electrodes, 5 mg of P3-SWNT carbon nanotube powder was dissolved in DI water by successive bath sonication (Crest CP360D, power level 9, 3 h) and probe sonication (VirTis VirSonic 100, 10 W, 5 min) followed by ultracentrifugation (13000 rpm, 1 h) to remove remaining agglomerations. Triton X-100 (0.1% wt) was finally added into the solution to facilitate the printing on PDMS. The ink for hybrid gate dielectric was prepared by first mixing PDMS (base only), $BaTiO_3$ nanoparticles, and 4-methyl-2-pentanone followed by magnetic stirring for 30 min. The mixture was then subjected to successive bath sonication (power level 9, 4 h) and probe sonication (15 W, 10 min) to break the large aggregations of $BaTiO_3$. The weights of PDMS and 4-methyl-2-pentanone were fixed at 1 and 4 g, respectively, while the weight of $BaTiO_3$ was varied from 0.5 to 2 g. Lastly, 0.3 g of curing agent was added to the dispersion before printing.

Device Fabrication. The surface of the PDMS substrate was rendered hydrophilic by O_2 plasma treatment (30 W, 500 mTorr, 3–5 s), followed by functionalization with poly-L-lysine (10 min). A semiconducting carbon nanotube network was then deposited by drop-casting for 30 min. The substrate was then rinsed with deionized water to remove excessive surfactant followed by blow dry with N_2. Source/drain electrodes (usually ~200–300 μm wide) were subsequently patterned by printing P3-SWNT solution on the

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substrate for 40−50 layers at 60 °C using a Sonoplot Microplotter equipped with micropipettes with ∼100−150 μm openings. The TFT channels were then defined by patterning the sSWCNT network by O_2 plasma etching (60 W, 40 s) with the channel protected by printed S1813. After S1813 was removed by acetone rinsing, PDMS/$BaTiO_3$ gate dielectric was subsequently printed and cured at 150 °C for 20 min. Finally, P3-SWNT ink was printed on top of the gate dielectric layer for 20−30 layers at 60 °C as the top gate electrode. This concludes the fabrication of stretchable TFTs. For the logic circuits, P3-SWNT ink was printed into the channel region of the load resistor in a layer by layer fashion until an optimal resistance value was achieved. After all components were printed and the desired performance was achieved, a PDMS layer was printed as the encapsulant.

Characterizations. The electrical characteristics of TFTs and logic gates were measured by an Agilent B1500A semiconductor parameter analyzer. Resistance of the printed CNT electrodes was measured by a Keithley 2100 multimeter controlled by a LabView program. The gate dielectric layer material was characterized by the CV module (B1520A) of the Agilent B1500A analyzer. Stretching tests were performed automatically with a syringe pump. Scanning electron micrographs, atomic force micrographs, and optical micrographs were captured with a Hitachi S-4700II field emission scanning electron microscope (FESEM), a Dimension 3100 atomic force microscope (AFM), and an Olympus BX51 optical microscope, respectively. All measurements were conducted under ambient conditions.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b07190.

Details about the fabrication processes of the fully printed, stretchable TFTs, and integrated logic circuits and additional experimental details (S1−S14) (PDF)

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Author Contributions

L.C. and C.W. conceived the idea and designed the experiments. L.C carried out the material and recipe development, device fabrication, and electrical characterization. L.C. and Z.Y. contributed to the preparation of $BaTiO_3$/PDMS dispersions. L.C., S.Z., J.M., and C.W. contributed to the data analysis. L.C. and C.W. wrote the paper, and all authors provided feedback.

Notes

The authors declare no competing financial interest.

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