IOP Publishing Nanotechnology
Nanotechnology 28 (2017) 435203 (11pp) https://doi.org/10.1088/1361-6528/aa87fa

Designing hybrid gate dielectric for fully printing high-performance carbon nanotube thin film transistors

Qian Li[1,2], Shilong Li[1,2,3], Dehua Yang[1,2,3], Wei Su[1,2,3], Yanchun Wang[1,2], Weiya Zhou[1,2], Huaping Liu[1,2,4,5] and Sishen Xie[1,2,4]

[1] Beijing National Laboratory for Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, Beijing 100190, People's Republic of China
[2] Beijing Key Laboratory for Advanced Functional Materials and Structure Research, Beijing 100190, People's Republic of China
[3] University of Chinese Academy of Sciences, Beijing 100049, People's Republic of China
[4] Collaborative Innovation Center of Quantum Matter, Beijing 100190, People's Republic of China

E-mail: liuhuaping@aphy.iphy.ac.cn and ssxie@iphy.ac.cn

Received 5 June 2017, revised 18 August 2017
Accepted for publication 23 August 2017
Published 2 October 2017

Abstract

The electrical characteristics of carbon nanotube (CNT) thin-film transistors (TFTs) strongly depend on the properties of the gate dielectric that is in direct contact with the semiconducting CNT channel materials. Here, we systematically investigated the dielectric effects on the electrical characteristics of fully printed semiconducting CNT-TFTs by introducing the organic dielectrics of poly(methyl methacrylate) (PMMA) and octadecyltrichlorosilane (OTS) to modify SiO_2 dielectric. The results showed that the organic-modified SiO_2 dielectric formed a favorable interface for the efficient charge transport in s-SWCNT-TFTs. Compared to single-layer SiO_2 dielectric, the use of organic–inorganic hybrid bilayer dielectrics dramatically improved the performances of SWCNT-TFTs such as mobility, threshold voltage, hysteresis and on/off ratio due to the suppress of charge scattering, gate leakage current and charge trapping. The transport mechanism is related that the dielectric with few charge trapping provided efficient percolation pathways for charge carriers, while reduced the charge scattering. High density of charge traps which could directly act as physical transport barriers and significantly restrict the charge carrier transport and, thus, result in decreased mobile carriers and low device performance. Moreover, the gate leakage phenomenon is caused by conduction through charge traps. So, as a component of TFTs, the gate dielectric is of crucial importance to the manufacture of high quality TFTs from the aspects of affecting the gate leakage current and device operation voltage, as well as the charge carrier transport. Interestingly, the OTS-modified SiO_2 allows to directly print horizontally aligned CNT film, and the corresponding devices exhibited a higher mobility than that of the devices with the hybrid PMMA/SiO_2 dielectric although the thickness of OTS layer is only ~2.5 nm. Our present result may provide key guidance for the further development of printed nanomaterial electronics.

Supplementary material for this article is available online

Keywords: carbon nanotubes, thin-film transistors, hybrid gate dielectric, fully printing, high performance

(Some figures may appear in colour only in the online journal)

[5] Author to whom any correspondence should be addressed.

1. Introduction

Single-wall carbon nanotube (SWCNT) thin-film transistors (TFTs) have been extensively studied due to their extremely high mobility, low operation voltage and high operation speed [1–7]. Compared to single-SWCNT transistors, SWCNT-TFTs could output a much higher work current and power. SWCNT-TFTs have previously been fabricated by a complicated photolithography and lift-off process [8–10]. Recently, the fabrication of SWCNT-TFTs by ink-printing SWCNT solution at a well-defined position on a substrate was reported, which dramatically simplified the fabrication process [11–14]. The performance of the ink-printed SWCNT-TFTs is strongly dependent on the electronic purity of the semiconducting nanotube ink. The presence of metallic SWCNTs could shortcut the source and drain electrodes, degrading the device performance. Recently, several sorting methods of SWCNT structures including density gradient ultracentrifugation, ion-exchange chromatography and gel chromatography, have been reported [15–18], with which high-purity semiconducting SWCNT ink could be achieved.

In addition to high-purity semiconducting nanotube ink, the gate dielectric also plays an important role in achieving high-performance TFTs. A TFT can be regarded as a capacitor, where the gate insulator is sandwiched between the semiconductor layer and the gate electrode and, under the applied gate voltage and source-drain voltage, the injected charge carriers are attracted to the interface of the gate dielectric and semiconductor layer, where they form the source-drain current. In TFTs, charge carrier transport primarily occurs within the first few monolayes of the semiconductor films next to the gate dielectric, which is not only dependent on the microstructures of the semiconductor layer but is also strongly influenced by the surface properties of the gate insulator. So the first few semiconducting layers next to the dielectric interface are of vital importance because they dominate the charge carrier transport of the device. The dependence of TFT response characteristics on dielectric roughness can attribute to three factors. First, the efficient percolation pathways for charge carriers is dramatically reduced by the higher dielectric roughness severely limiting the migration of charge carriers. Second, more trapping sites are induced by higher roughness. The obvious consequence of the transport through traps in the devices is the higher level of leakage current. Finally, the charge carrier transport is hindered by surface scattering effects caused by the surface roughness. Moreover, the hysteresis phenomenon is mainly attributed to the charge trapping at the semiconductor-dielectric interfaces, it will be noticeable in transfer curves due to high trap density at the dielectric interface. Therefore, generally speaking, the gate dielectric should have low leakage current, minimum density of surface carrier traps and smooth surface for efficient charge carrier transport, which thus ensures high device performance. However, inorganic dielectrics usually induce interfacial scattering and trapping of carriers [19, 20], and undermines the performance of transistors. The combination of inorganic and organic layers to create hybrid gate dielectrics that provide a smooth surface, a small surface energy and negligible gate leakage has been reported in the fabrication of organic TFTs [21–23]. Such hybrid bilayer dielectrics are generally composed of an inorganic metal oxide layer, ideally one with a large dielectric constant (e.g., SiO_2, Al_2O_3, HfO_2), and an organic self-assembled monolayer (SAM) molecules or a layer of polymers. Such hybrid gate structure can significantly improve the crucial performance parameters of the devices, and it can be exploited to tune the threshold voltage of the TFTs [24–28], produce low-voltage operating TFTs [29], control the charge-carrier density [24], and reduce the gate leakage current [30]. However, the application of the inorganic–organic hybrid gate dielectric in the SWCNT thin film transistors is still poorly explored.

In this presentation, we investigated the effect of dielectrics on the performances of SWCNT thin film transistors fabricated by fully printing technique. PMMA and OTS were chosen for their diverse dielectric constants. All s-SWCNT-TFTs with polymer dielectrics show typical p-type charge transport and high on/off ratios. The present results show that the use of organic–inorganic hybrid bilayer dielectrics reduces charge trapping and leakage current, leading to a clear improvement in the SWCNT-TFT performance including high field-effect mobility, large on–off ratio, low threshold voltages and small hysteresis. Especially, the OTS gate insulator layer clearly induced the orientation arrangement of the printed SWCNTs and improved the carrier mobility of the CNT-TFTs due to the suppression of charge scattering by the CNT–CNT junctions. Our present work provides a new way for fabricating high-performance SWCNT TFTs, accelerating the application of SWCNTs in micro-devices.

2. Methods

2.1. Preparation of PMMA/SiO_2 dielectric

The PMMA/SiO_2 hybrid dielectric was prepared by spin-coating PMMA solution on a heavily-doped n-type silicon wafer ($\rho = 0.01\ \Omega$ cm) with an oxide thickness of 500 nm, which was oxidized by oxygen plasma. Before the deposition of the PMMA layer, the SiO_2/Si substrates were ultrasonically cleaned in acetone and ethanol and then dried by N_2. A solution 0.4 wt% of PMMA ($M_n = 495$, Aldrich) intoluene was spin-coated at 4000 rpm on the SiO_2 layer for 60 s and then baked at 180 °C for 1 min on a hot plate. The thickness of PMMA confirmed to be about 100 nm by atomic force microscopy (AFM, Multimode 8, Bruker).

2.2. Preparation of hybrid OTS/SiO_2 dielectric

To make a hybrid dielectric of OTS/SiO_2 for bottom gate devices. OTS (Aldrich Co., Ltd) was prepared with a concentration of 2.5×10^{-4} M in a solvent mixture of 1:3 volume cyclohexane/chloroform. The cleaned substrates (SiO_2/Si) were immersed into the solution of OTS for a time. After adsorption, the OTS-coated substrates were washed

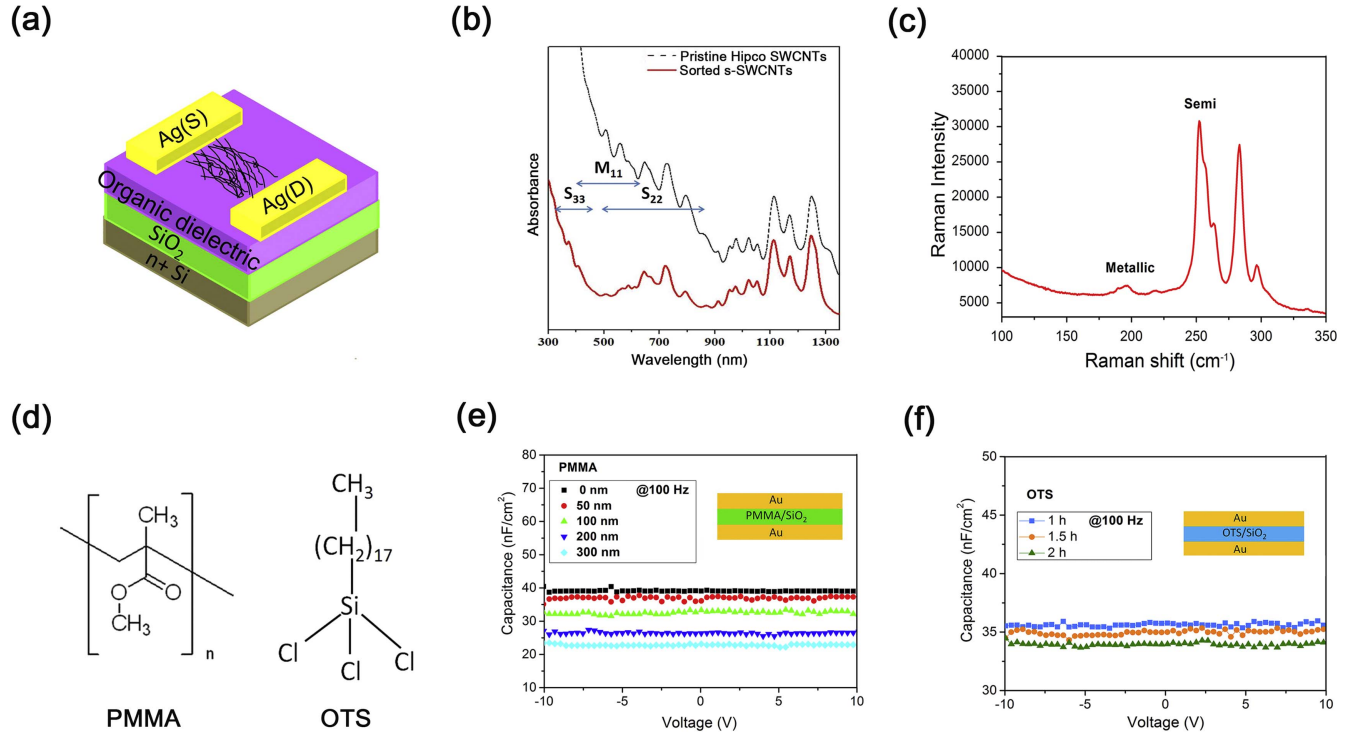

Figure 1. (a) Schematic illustration of the layout of the printed thin-film transistors. (b) Optical absorption spectra and (c) Raman characterization of the semiconducting SWCNT ink. (d) The chemical structures of the organic dielectrics PMMA and OTS (e) and (f) present the capacitance–voltage (C–V) characteristics of PMMA/SiO_2 and OTS/SiO_2 hybrid dielectrics, respectively. The insets in (e) and (f) show the schematic diagram of the metal–insulator–metal (MIM) structure for the measurement of the dielectric capacitance.

with chloroform for 30 min in an ultrasonic bath to remove the redundant silane deposits, rinsed in deionized (DI) water and then dried with blowing nitrogen.

2.3. Fully printing SWCNT-TFTs

An aqueous solution of semiconducting SWCNTs with 0.5 wt% sodium deoxycholate separated from HiPco-SWCNTs (diameter 0.7–1.1 nm) with the gel chromatography technique was used as SWCNT electronic ink [17] (see the details in the supporting information S1 is available online at stacks.iop.org/NANO/28/435203/mmedia). Ink-printing of SWCNTs and Ag electrodes was performed using a Sonoplot GIX Microplotter II as the following steps: (a) SWCNT channel film was printed with a 30 μm tip. The channel length and width are 100 and 500 μm, respectively. The procedure was repeated twice. Then, they were aged overnight and subsequently rinsed with DI water to remove the surfactant residue in the SWCNT film; (b) silver source-drain electrodes with 1 mm^2 were printed using a 10 μm tip; (c) the devices were annealed in air at 100 °C for 30 min to improve the contact of the SWCNT thin films and electrodes.

The optical absorption spectra of the SWCNT ink were recorded by an UV–vis-NIR spectrophotometer (Shimadzu, UV-3600). The topography of the SWCNT films was characterized using AFM (Multimode 8, Bruker). The electrical characterizations of the TFTs were recorded using a Keithley4200 semiconductor characterization system. The capacitance values of the dielectrics were measured utilizing an electrochemical workstation (CH Instruments model CHI601C).

3. Results and discussions

The bilayer hybrid dielectric configuration for SWCNT-TFTs is depicted in figure 1(a). All SWCNT-TFT elements including Ag electrodes and channels are ink-printed on the substrates without involving any photolithography patterning or surface pretreatment steps. The channel length and width were fixed at 100 and 500 μm, respectively. Figure 1(b) shows the UV–vis-NIR absorption spectra of the as-prepared semiconducting SWCNT inks (red trace), which evidences that the inks are high-purity semiconducting SWCNTs (s-SWCNTs) due to the lack of metallic M_{11} peaks. The purity was evaluated around 99% by the ratio of the relative area under the metallic and semiconducting peaks [31, 32]. Raman spectrum further confirmed the absence of metallic tubes in the s-SWCNT ink (figure 1(c)). The chemical structures of the organic dielectrics PMMA and OTS are presented in figure 1(d). The capacitance−voltage (C−V) characteristics of the hybrid dielectrics PMMA/SiO_2 and OTS/SiO_2 were measured by using the metal–insulator–metal structure [33] (the insets in figures 1(e) and (f)) and sweeping from −10 V to +10 V at 100 Hz. The growth process of OTS self assembled molecular film is 'island' growth mode by solution chemical method. Monolayer is very sensitive to reaction time, different results will be obtained under different

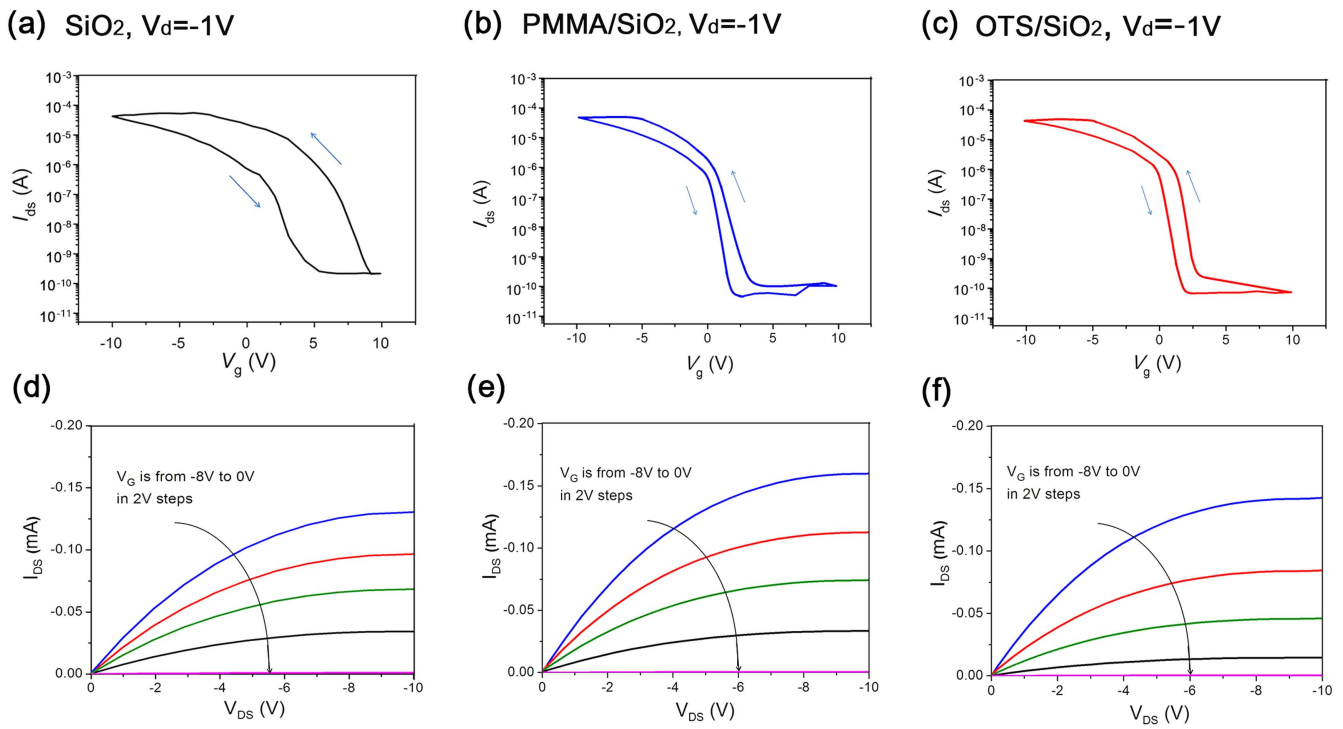

Figure 2. Electrical performances of SWCNT-TFTs with various dielectrics. (a), (b), (c) Transfer characteristics of the SWCNT devices with single SiO_2 of 500 nm, PMMA/SiO_2 and OTS/SiO_2 dielectrics at $V_{DS} = -1$ V. (d), (e), (f) Output characteristics with V_G ranging from −8 to 0 V with a step of 2 V (top to bottom). The thickness of PMMA layer is 100 nm. The OTS layer by immersion for 2 h is about 2.5 nm. The channel lengths (L) and widths (W) of SWCNT-TFTs were fixed at 100 and 500 μm, respectively.

time, so the OTS-SAM film possessed different thickness with various amounts of time. Therefore, we measured the thickness of OTS/SiO_2 based on various immersion time in an OTS solution. As shown in figures 1(e) and (f), the capacitance per unit area is almost constant over the entire voltage range for both PMMA/SiO_2 and OTS/SiO_2 hybrid dielectrics. With an increase in the thickness of organic dielectrics, the capacitance clearly decreased.

Figure 2(a) shows the typical transfer characteristics of the s-SWCNT-TFTs fabricated with single SiO_2 dielectric layer of 500 nm (source/drain voltage, $V_{DS} = -1$ V). It is clear that the TFTs are p-type with a current on–off ratio (I_{on}/I_{off}) of $\sim 10^5$. The mobility (μ_{device}) of the devices is about 51 $cm^2\,V^{-1}s^{-1}$ under the drain voltage of −1 V, which were calculated from the following equation:

$$\mu_{device} = \frac{L}{V_{DS} C_i W} \cdot \frac{dI_{DS}}{dV_G} = \frac{L}{V_{DS} C_i} \cdot \frac{g_m}{W}, \qquad (1)$$

where L and W are the device channel length and width, g_m is the maximum transconductance which is extracted by taking the derivative of the transfer characteristics. C_i is the capacitance per unit area of the hybrid dielectrics. For comparison, we fabricated SWCNT-TFTs with PMMA/SiO_2 and OTS/SiO_2 hybrid dielectrics and characterized their electrical properties (figure 2(c)), in which PMMA layer is 100 nm and OTS is ~2.5 nm. It is clear that the TFTs are p-type with a current on–off ratio (I_{on}/I_{off}) of $\sim 10^6$. The mobility (μ_{device}) of the devices reaches 81 $cm^2\,(V^{-1}\,s^{-1})$ (PMMA/SiO_2) and 90 $cm^2\,(V^{-1}\,s^{-1})$ (OTS/SiO_2) under the drain voltage of −1 V, which is clearly higher than that of the unmodified devices. We compared the threshold voltage (V_{th}) of various transistors, the V_{th} for the SWCNT-TFTs with single SiO_2 dielectric layer is 6.5 V, while those of the devices with PMMA/SiO_2 and OTS/SiO_2 hybrid dielectrics decreased rapidly and the values are 2.6 V and 2.1 V, respectively. The subthreshold slope (SS), which describes the turn on of the TFTs, is another measure of device quality, and is defined by $SS = \frac{dV_G}{d(\log I_{DS})}$. On the basis of the transfer characteristics of the TFTs in figure 2, the calculated SS for the SWCNT TFTs with the PMMA and OTS modified gates are 800 and 760 mV/decade, while that of the devices with single SiO_2 gate dielectrics is 1000 mV/decade.

A large hysteresis at sweep cycling for the transfer characteristics is one of the main problems in s-SWCNT-TFTs [34, 35], which derived from the interface traps between the s-SWCNTs and dielectric, as well as the bulk traps in the gate dielectrics [34–36]. The hysteresis can be evaluated quantitatively by the difference between two V_g at the center of the maximum and minimum drain currents for forward and reverse gate-voltage sweeping [37]. The hysteresis of the devices using the hybrid dielectrics of PMMA/SiO_2 and OTS/SiO_2 are approximately 1.8 and 2 V while that of the devices with single SiO_2 is approximately 5 V. The decreased hysteresis in the organic-modified SWCNT-TFTs should be due to the suppression of charge trapping by the organic dielectric. We will discuss this issue later.

Figures 2(d)–(f) delineates the well-behaved output characteristics for the devices with different dielectrics. The I_{DS} shows a linear increase with V_{DS} between −1 and 0 V,

Table 1. Summary of the device performance of SWCNT-TFTs with bare SiO_2 and bilayer dielectrics.

Dielectric	V_{th} (V)	g_m (μS)	μ ($cm^2\,V^{-1}\,s^{-1}$)	I_{on}/I_{off}	SS (mV/dec)
SiO_2	6.5	11.1	53	7.1×10^5	1000
$PMMA/SiO_2$	2.6	13.6	85	6.5×10^6	800
OTS/SiO_2	2.1	15.3	91	3.1×10^6	760

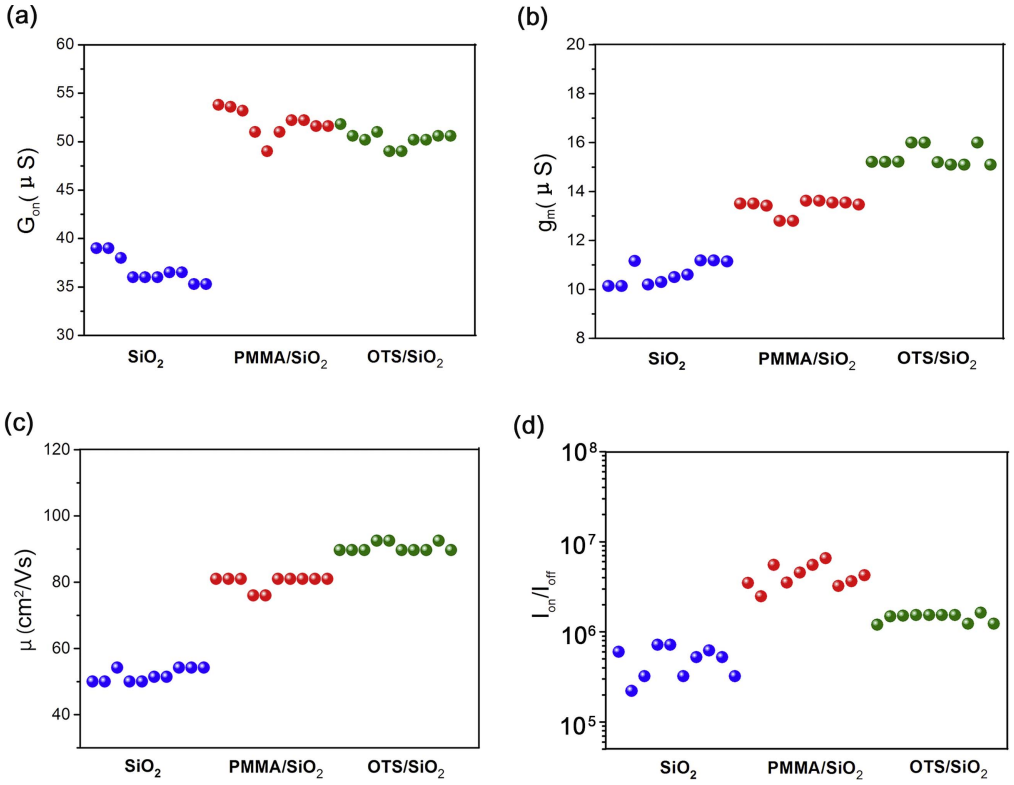

Figure 3. The distribution of electrical performances of 10 SWCNT-TFTs with single SiO_2 dielectric (blue), 10 SWCNT-TFTs with PMMA (100 nm)/SiO_2 hybrid dielectric (red) and 10 SWCNT-TFTs with OTS/SiO_2 hybrid dielectric (OTS SAMs formed by 2 h) (green). The channel length and width for all devices are 100 μm and 500 μm, respectively. (a) On-conductance, (b) transconductance, (c) device mobility, and (d) on–off current ratio.

and with further increasing the V_{DS}, the I_{DS} curve shows saturation behavior. The CNT-TFT devices with organic–inorganic hybrid dielectrics offer larger output current (0.17 mA for $PMMA/SiO_2$; 0.15 mA for OTS/SiO_2) even under low-operation voltage (at $V_G = -8$ V and $V_{DS} = -10$ V) (figures 2(d) and (e)) than that of single SiO_2 dielectric (0.12 mA). Detailed characteristics of the devices are reported in table 1.

For fully investigating the effect of the hybrid dielectrics on the device performances, we compared the electrical properties of 10 PMMA-modified SWCNT-TFTs and 10 OTS-treated SWCNT-TFTs with those of single SiO_2 dielectric devices. Their performances, including on-conductance, transconductance, field-effect mobility and I_{on}/I_{off} ratio, are summarized in figure 3 (also see table S1). Each of the performances for the organic-modified SWCNT-TFTs is higher than that of the devices with single SiO_2 gate dielectric. The off-current of the hybrid-gate devices is lower by an order of magnitude (figure S2), which contributes to a higher I_{on}/I_{off} ratio.

In order to fabricate high-speed integrated digital circuits, each transistor should concurrently have high mobility and I_{on}/I_{off} ratio. As shown in figure 4(a), the devices with bilayer hybrid gate dielectrics show consistently higher mobility and I_{on}/I_{off} ratio compared to that without modification, exhibiting much better performances. We also compared the performances of the PMMA and OTS modified devices with those of a few recently reported SWCNT-TFTs with single SiO_2 dielectric [11–13, 26, 38–40]. As shown in figure 4(b) (also see table S2), the mobility and I_{on}/I_{off} ratio of our SWCNT-TFTs (control devices) with hybrid dielectric are significantly better than those of the devices recently reported in the literatures.

Since we used identical channel materials, substrates and metal electrode in this work, the improved performances of the organic-modified devices should be ascribed to their hybrid gate dielectrics. We first investigated the surface morphologies of the untreated and modified SiO_2 substrates using AFM (figure 5). As shown in figures 5(a) and (d), the surface of pristine SiO_2 is very rough. After the deposition of

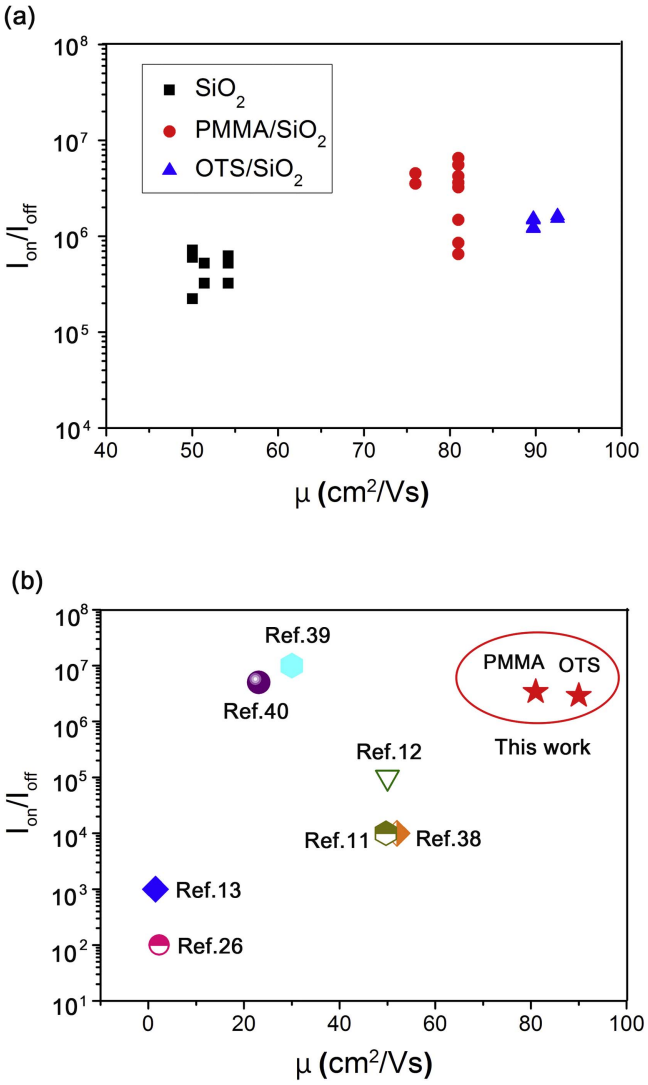

Figure 4. (a) Comparison of a few recent solution-processed CNT devices with one SiO_2 dielectric layer. (b) On–off current ratio versus mobility of all the devices with organic-modified gate dielectrics and single SiO_2 dielectric. The thickness of PMMA layer is 100 nm. OTS SAMs formed by 2 h. In all the devices, the channel length and width are 100 μm and 500 μm, respectively. Both the mobility and on–off current ratio of the modified devices are higher than that without modification.

organic dielectric, both PMMA/SiO_2 (figures 5(b), (e) and S3) and OTS/SiO_2 (figures 5(c), (f) and S4) hybrid dielectrics shows smooth surfaces. The analysis of the substrate surface roughness indicated that the RMS roughness of the pristine SiO_2 surface is around 4.27 nm, while those of the PMMA/SiO_2 and OTS/SiO_2 films are 0.27 and 0.15 nm, respectively. According to the multiple-trap-release model, higher channel charge is accompanied with a better free charge to total charge ratio, leading to improvement in field effect mobility [41]. On SiO_2 dielectric surface with a high roughness, there will be a lot of defects in the interface, when the carrier injection from the source, these will be trapped, and due to the rough surface of the substrate, resulting in carrier scattering enhancement, which will reduce the field-effect mobility of the device. In addition, V_{th} for the transistor is referred to charge trapping and the effect of surface scattering at the interface of dielectric/semiconductor layer. In TFTs operating above threshold, most of the charge induced by the gate-source voltage is trapped in the numerous traps and only a fraction of the carriers participates in the current conduction, which lead to a high V_{th}. A better explanation can be found, if we consider the holes located in roughness 'valleys' at the dielectric. The source-drain field only supports drift movement along the surface and cannot support a charge movement out of the roughness valley away from the surface, the more charges are trapped at the interface, the stronger gate voltage is needed to turn the transistor on. The deposition of a PMMA layer and OTS-SAM film effectively passivates charge traps and generates more pathways for the charge carriers thus benefits the charge transport and obviously decreases the V_{th}. Moreover, on dielectric surfaces with a high density of trap states, more mobile holes are trapped and do not make contribution to the drain current of the unmodified SiO_2 device in the same time scale, which lead to a decreased drain current. Besides, the leakage current density of the device is relatively high due to induced charge trap by the roughness valleys [42]. The presence of charge traps in the insulator will generally result in a greatly reduced current at lower injection levels, since those traps initially empty will capture, and thereby immobilize, most of the injected carriers. The equilibrium trap occupancy results from a balance between capture of electrons into the traps, the electrons will contribute to the current flow through the insulator. So the contribution of the charge traps to the gate leakage current cannot be ignored. Moreover, the current hysteresis originates from the interface traps distributed between s-SWCNTs film and the dielectric, as well as the bulk traps in the gate dielectrics, which due to hole and electron trapping are explained as follows: (a) hole trapping—during OFF to ON state, holes get trapped at deep hole traps with increasing negative gate voltage which screen the applied gate voltage during reverse scan thereby reducing the effective gate voltage and hence causing reduced drain current, (b) electron trapping-electrons trapped, especially at the dielectric/semiconductor interface, under positive gate voltages during off to on state scan induces additional holes at the interface. Furthermore, the difference in SS approximately reflects the trapping and defect density of the dielectric layer [43].

Interestingly, the morphologies of the printed SWCNT films on different dielectrics are different. As shown in figures 5(g) and (h), the printed SWCNT films on the untreated SiO_2 and PMMA/SiO_2 are random network without any alignment. In contrast, the printed SWCNT film on the OTS/SiO_2 gate dielectric exhibits clear alignment (figure 5(i)). Organic OTS was widely used for the modification of substrates to prevent the adsorption of SWCNTs due to the weak interaction between the surfactant-encapsulated SWCNTs and OTS layer [44]. Here, we found that the OTS organic layer could induce the alignment of SWCNTs. The detailed reason is still unclear. We propose that the interaction between SWCNTs and OTS dielectrics should play a critical role in the orientation arrangement of SWCNTs. For SWCNT network film, the number of

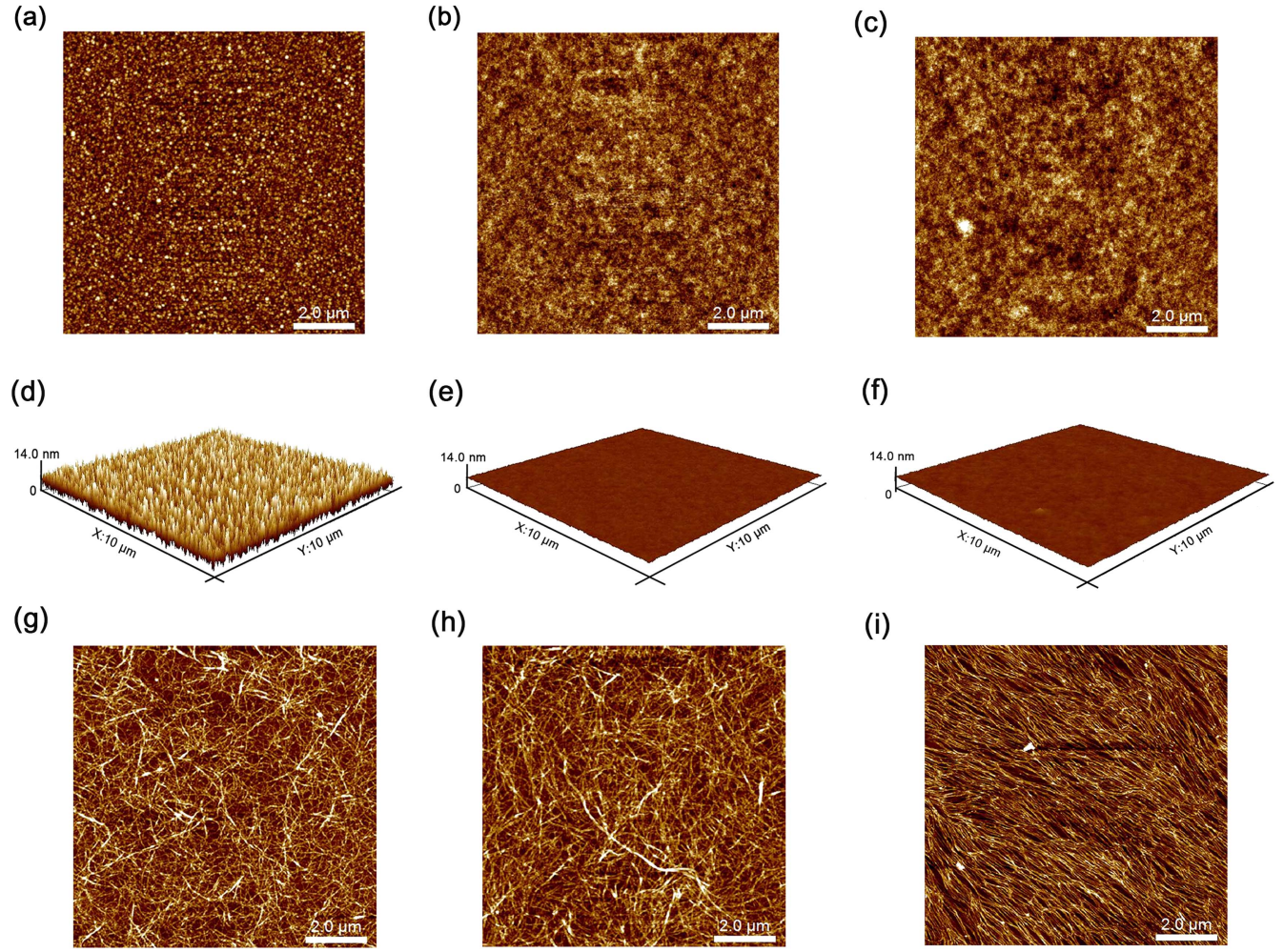

Figure 5. AFM images (10 μm × 10 μm) of (a), (d) SiO_2 dielectric layer; (b), (e) PMMA (100 nm)/SiO_2 dielectric layer; (c), (f) OTS/SiO_2 dielectric layer (OTS SAMs formed by 2 h). SWCNT film printed on (g) SiO_2 dielectric layer; (h) PMMA/SiO_2 dielectric layer; (i) OTS/SiO_2 dielectric layer.

tube-to-tube junctions, which limits the charge transport through the film because of the carrier scattering through tube-to-tube junctions [45–47], can be reduced by controlling the alignment of SWCNTs, thereby improving the mobility of the device. The improved physical contact between carbon nanotubes increases the overall electrical conductivity of the channel during charge accumulation in the 'on' state, thus, would lead to smaller values of SS for OTS-treated TFTs. Moreover, the low SS is indicate a high quality OTS/SWCNT interface compared with PMMA/SiO_2 and unmodified SiO_2. OTS-SAMs on the dielectric layer could also be a useful buffer layer effectively passivating the charge traps, especially the interfacial electron traps induced by the -OH groups on the SiO_2 surface, for efficient charge carrier transport [48, 49]. Due to the hydrophilic surface, the bare SiO_2 is easy to absorb water molecules which usually behave as traps in the devices. The OTS-SAM-modified strongly hydrophobic dielectric surface should adsorb only small amounts of water, the reduction of hydroxyl groups and water molecules on the modified dielectric surface enhanced the performance of the devices significantly. By reduced charge transfer, such as surfactants and/or water molecules (oxygen), absorbed on the surface of the SWCNTs, the TFTs with OTS-SAM exhibit relatively low V_{th} in comparison with devices with PMMA/SiO_2 and bare SiO_2.

The charge-trap densities in the device channels can be further calculated using the following equation [50]:

$$D_{tr} = \frac{C_i}{q}\left[\mathrm{SS}\frac{\log(e)}{kT/q} - 1\right], \qquad (2)$$

where SS is the subthreshold slope, q is the electronic charge, C_i is the capacitance per unit area, k is the Boltzmann's constant, and T is the absolute temperature. The D_{tr} of the devices with single SiO_2 is $0.68 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$, while the devices with PMMA/SiO_2 and OTS/SiO_2 dielectrics are 0.41×10^{12} and $0.48 \times 10^{12}\,\mathrm{cm^{-2}\,eV^{-1}}$ respectively. The SWCNT-TFTs with organic-modified dielectrics have lower charge-trap densities for holes. Higher interface charge-trap density on SiO_2 substrates likely results from hydroxyl groups and/or physical defects on their surfaces.

In order to further investigate the role of organic dielectric in improving the performances of SWCNT devices, the leakage current of the SiO_2, PMMA/SiO_2 and OTS/SiO_2 gate dielectrics were measured by preparing a simple symmetrical structure

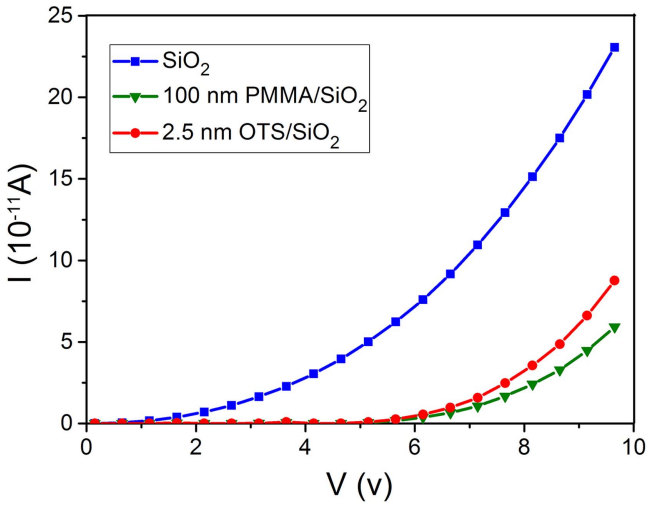

Figure 6. Leakage currents for SiO_2, PMMA/SiO_2 and OTS/SiO_2 dielectrics. The PMMA thickness is 100 nm and that of OTS layer 2.5 nm.

(Ag/SiO_2/doped Si/Ag, Ag/PMMA/SiO_2/doped Si/Ag and Ag/OTS/SiO_2/doped Si/Ag), as shown in figure S5. Figure 6 shows the current as a function of voltage. The result indicates that the introduction of a PMMA and OTS layer on the surface of SiO_2 dielectric reduced the leakage current by three times than that of single SiO_2 dielectric. We think that the plasma-grown SiO_2 dielectric without modified has very poor insulating property, the modification of organic PMMA and OTS significantly enhance the insulation performance of dielectric. Compared with the unmodified single SiO_2, the hybrid bilayer dielectrics exhibit a relatively low leakage current. These results are well consistent with the small off-current of the PMMA and OTS-SAM modified devices (supporting information, figure S1). In comparison, note that the test structures including an OTS-SAM exhibit a very low gate leakage current (~0.8 pA) under the 9.8 V which is comparable with that of the PMMA/SiO_2 gate dielectric despite its much smaller thickness of ~2.5 nm. This confirms the crucial role of the SAM in determining the insulating properties of the dielectric stack, despite its small thickness. A similar conclusion has previously been drawn for organic SAM-containing sandwich devices [51, 52].

We systematically explored the effect of PMMA thickness on the performances of SWCNT-TFTs, in which channel length and width are fixed at 100 and 500 μm. The dielectric properties of PMMA/SiO_2 gate dielectric are exhibited in figure 1(d). Small capacitance per unit area and dielectric constant inevitably lead to a decrease in the production of carriers under the same gate voltage and thus small on-currents. Therefore, with an increase in the thickness of PMMA dielectric, we measured decreased on-currents (figure 7(a)), which negatively contributes to the on/off ratio. Figure 7(a) shows that the on–off ratio increases rapidly with an increase in PMMA layer thickness from 50 to 100 nm. With a further increase in PMMA thickness, I_{on}/I_{off} nearly remains at a constant (around 10^6). In addition, we investigated the leakage current of the PMMA/SiO_2 gate dielectrics as a function of the thickness of PMMA layer (supporting information, figure S6). With an increase in the thickness of PMMA layer to 100 nm, leakage current decreases rapidly to $\sim 10^{-11}$ A, indicating that a reduction in low leakage current by hybrid gate dielectric mainly contributes to the increased I_{on}/I_{off} ratio of SWCNT-TFTs. However, a further increase, especially from 200 to 300 nm, in the thickness of PMMA layer does not lead to a clear reduction in the leakage current, indicating that 200 nm is the optimized thickness for preventing leakage current. Figure 7(b) shows transconductance (g_m), field-effect mobility (μ), and the subthresholdslope (SS) of the SWCNT-TFTs as a function of PMMA thickness. Each feature is optimal for the devices with 100 nm thick PMMA dielectric. The field-effect mobility increases with a reduction in the thickness of PMMA dielectric. This trend can be explained by the multiple trap and release model [43], in which the field-effect mobility is dependent on the ratio of the free carriers to total carriers. The relationship can be expressed as:

$$\mu = \mu_b \times \frac{n_f}{n_t + n_f}, \quad (3)$$

where μ_b represents the mobility near the majority-carrier transport band (i.e., conduction band or valence band, depending on whether one is dealing with an n- or p-type semiconductor), n_f and n_t are free and trapped carrier density at the semiconductor/insulator interface. As gate voltage increases, the ratio of free to trapped carrier density increases, resulting in increased mobility. The similar effect could occur with increasing dielectric capacitance while keeping gate voltage unchanged. In the present work, an increase in dielectric capacitance resulted from a reduction in PMMA thickness likely induces a higher ratio of the free carrier density to total carriers and thus higher field effect mobility. Similarly, SS and g_m of the devices are also strongly related to the gate dielectrics and capacitances [53]. A higher gate dielectric constant usually endows the devices small SS and large g_m. This is why the devices with 100 nm thick PMMA dielectric exhibit a smaller SS and higher g_m, compared to the thicker PMMA dielectric. However, a further decrease in the PMMA thickness from 100 to 50 nm leads to a dramatic increase in gate leakage current and degrades the performances of devices. Here, 100 nm PMMA layer is the optimized thickness for fabricating high-performance TFTs. We also measured the roughness of the PMMA dielectrics with various thickness. The surface of 100 nm thick PMMA with a roughness of 0.27 nm is the smoothest (as shown in figures S3, S7 and S8), the smooth dielectric layer create sufficient pathways for charge carriers, favor effective carrier transport, while reduced the charge scattering, which contributes to the high performances of devices. Conversely, rough dielectric surfaces will lead to a high density of trap states and, stronger surface scattering effects on charge carriers will resulted in a reduction in charge carrier mobility and the increase of leakage current density. Synthesizes the above-mentioned factors, the device with 100 nm PMMA/SiO_2 dielectric possesses optimal transistor performance.

The effect of the morphologies of the OTS organic layer on the performances of the printed SWCNT-TFT devices was

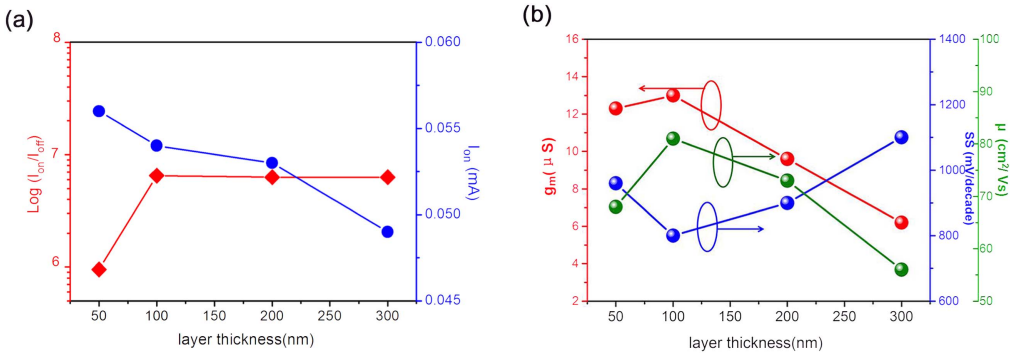

Figure 7. Effect of the thickness of PMMA dielectric on the electrical properties of SWCNT-TFTs. (a) Average on-current I_{on} and on/off ratio ($\log(I_{on}/I_{off})$) as a function of PMMA thickness. (b) g_m, subthreshold slope (SS) and field-effect mobility (μ) as a function of PMMA thickness.

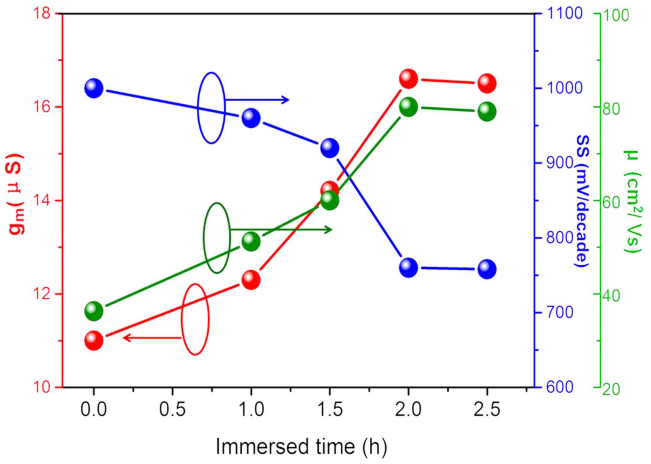

Figure 8. Electrical properties of SWCNT-TFTs with OTS/SiO_2 dielectric layer as a function of various dipping time for a certain OTS concentration. In all devices, the channel length and width are 100 μm and 500 μm, respectively.

also investigated. Figure S9 presents typical AFM images of the surfaces of the as-prepared OTS/SiO_2 hybrid dielectrics by immersing a freshly SiO_2/Si into OTS solution for varied time. The growth process of OTS SAM film is 'island' growth mode. Area of the OTS-SAM coverage gradually increased with the treatment time and the complete OTS monolayer was formed after immersion for 2 h. With an increase in the immersion time, the average roughness R_a of the OTS/SiO_2 layer is 0.283 nm, 0.202 nm and 0.119 nm for immersion time of 0.5, 1 and 2 h. As the SiO_2/Si surface was covered by OTS monolayer, the surface roughness decreased with increasing immersion time. When a complete monolayer was formed, the roughness was very small and the film has a smooth compact morphology. By introducing OTS SAM-SiO_2 bilayers dielectric, the surface quality of OTS/SiO_2 dielectric was significantly increased and the leakage current was reduced, thus leading to improved performances of the SWCNT-TFTs.

We characterized the variation of the electrical properties of the devices as a function of immersion time for the same OTS concentration. As shown in figure 8, the transistor performances were improved at the initial stage and leveled off with immersion time. The mobility of the device reached 90 $cm^2\,V^{-1}\,s^{-1}$ when uniform OTS film was formed after immsion for 2 h. With further increasing the treatment time, the thickness of the OTS-SAM remains basically unchanged at the 2–3 nm level (supporting information figure S10), the electrical properties of the OTS-modified devices kept unchanged afterwards [54] and approached to a steady state. In other words, the optimized treat time of SiO_2 substrates in OTS solution for the prepartion of OTS/SiO_2 should be 2 h.

4. Conclusions

Generally, the semiconductor/dielectric interface plays a special role on the charge transport properties because the field-effect current mainly locates in the first few monolayers of the semiconducting layer near to the gate dielectric. Dielectric surface roughness was found to drastically decrease the electrical performances of TFTs, which can be attributed to an increasing amount of trap states, surface scattering, as well as the hindering of the movement of charges by the roughness valleys on dielectric surfaces. While the gate leakage current results from the conduction of electrons in the traps. Modification of this interface therefore offers a general way to improve carrier transport accordingly. We fabricated high-performance fully printed CNT-TFTs by using PMMA/SiO_2 and OTS/SiO_2 inorganic–organic bilayer as gate dielectrics, which reduced charge trapping, carrier scattering and gate leakage. The optimized thicknesses of PMMA and OTS are 100 and ~2.5 nm.

More importantly, we discover that OTS monolayer on SiO_2 efficiently induced the orientation arrangement, which could reduce the junction–junction scattering. The corresponding devices exhibit a higher mobility and smaller SS than those of the devices fabricated on PMMA/SiO_2 while keeping the on/off ratio at a high level of 10^6. The present result provides a new way to produce aligned SWCNT film and fabricate high-performance SWCNT-TFTs. This strategy has significant potential for applications in electronics, photoelectronics, and biosensor etc.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant No. 51472264, 11634014), and the Key Research Program of Frontier Sciences, CAS, Grant No. QYZDB-SSW-SYS028. Q.L. acknowledges the support by the China Postdoctoral Science Foundation (Grant No. 2016M591276). H. L. thanks the support by the Recruitment Program of Global Youth Experts and the '100 talents project' of CAS. The authors acknowledge Kailin Chi from Jilin University for his help in the capacitance measurement and Prof. Xuelei Liang from Peking University for his discussions. The authors are grateful for the support of Laboratory of Microfabrication, Institute of Physics, CAS.

References

[1] Kreupl F 2012 Electronics: carbon nanotubes finally deliver *Nature* **484** 321–2
[2] Cao Q, Han S-J, Tulevski G S, Zhu Y, Lu D D and Haensch W 2013 Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics *Nat. Nanotechnol.* **8** 180–6
[3] Appenzeller J 2008 Carbon nanotubes for high-performance electronics—progress and prospect *Proc. IEEE* **96** 201–11
[4] Kaskela A, Laiho P, Fukaya N, Mustonen K, Susi T, Jiang H, Houbenov N, Ohno Y and Kauppinen E I 2016 Highly individual SWCNTs for high performance thin film electronics *Carbon* **103** 228–34
[5] Chortos A *et al* 2016 Mechanically durable and highly stretchable transistors employing carbon nanotube semiconductor and electrodes *Adv. Mater.* **28** 4441–8
[6] Cao Y, Che Y C, Seo J-W T, Gui H, Hersam M C and Zhou C W 2016 High-performance radio frequency transistors based on diameter-separated semiconducting carbon nanotubes *Appl. Phys. Lett.* **108** 233105
[7] Brady G J, Joo Y, Roy S S, Gopalan P and Arnold M S 2014 High performance transistors via aligned polyfluorene-sorted carbon nanotubes *Appl. Phys. Lett.* **104** 083107
[8] Choi S-J, Bennett P, Lee D and Bokor J 2015 Highly uniform carbon nanotube nanomesh network transistors *Nano Res.* **8** 1320–6
[9] Liu N, Yun K N, Yu H-Y, Shim J H and Lee C J 2015 High-performance carbon nanotube thin-film transistors on flexible paper substrates *Appl. Phys. Lett.* **106** 103106
[10] Jang H-K, Jin J E, Choi J H, Kang P-S, Kim D-H and Kim G T 2015 Electrical percolation thresholds of semiconducting single-walled carbon nanotube networks in field-effect transistors *Phys. Chem. Chem. Phys.* **17** 6874
[11] Okimoto H, Takenobu T, Yanagi K, Miyata Y, Shimotani H, Kataura H and Iwasa Y 2010 Tunable carbon nanotube thin-film transistors produced exclusively via inkjet printing *Adv. Mater.* **22** 3981–6
[12] Lee C W, Pillai S K R, Luan X N, Wang Y L, Li C M and Chan-Park M B 2012 High-performance inkjet printed carbon nanotube thin film transistors with high-k HfO_2 dielectric on plastic substrate *Small* **8** 2941–7
[13] Zhao J W, Gao Y L, Gu W B, Wang C, Lin J, Chen Z and Cui Z 2012 Fabrication and electrical properties of all-printed carbon nanotube thin film transistors on flexible substrates *J. Mater. Chem.* **22** 20747–53
[14] Jang S, Kim B, Geier M L, Hersam M C and Dodabalapur A 2015 Short channel field-effect-transistors with inkjet-printed semiconducting carbon nanotubes *Small* **11** 5505–9
[15] Ghosh S, Bachilo S M and Weisman R B 2010 Advanced sorting of single-walled carbon nanotubes by nonlinear density-gradient ultracentrifugation *Nat. Nanotechnol.* **5** 443–50
[16] Tu X M, Manohar S, Jagota A and Zheng M 2009 DNA sequence motifs for structure-specific recognition and separation of carbon nanotubes *Nature* **460** 250–3
[17] Liu H P, Nishide D, Tanaka T and Kataura H 2011 Large-scale single-chirality separation of single-wall carbon nanotubes by simple gel chromatography *Nat. Commun.* **2** 309
[18] Zeng X, Hu J W, Zhang X, Zhou N G, Zhou W Y, Liu H P and Xie S S 2015 Ethanol-assisted gel chromatography for single-chirality separation of carbon nanotubes *Nanoscale* **7** 16273
[19] Veres J, Ogier S D, Leeming S W, Cupertino D C and Khaffaf S M 2003 Low-k insulators as the choice of dielectrics in organic field-effect transistors *Adv. Func. Mater.* **13** 199
[20] Yoon M-H, Kim C, Facchetti A and Marks T J 2006 Gate dielectric chemical structure–organic field-effect transistor performance correlations for electron, hole, and ambipolar organic semiconductors *J. Am. Chem. Soc.* **128** 12851
[21] Kumar A, Tyagi P, Dagar J and Srivastava R 2016 Tunable field effect properties in solid state and flexible grapheme electronics on composite high-low k dielectric *Carbon* **99** 579–84
[22] Ortiz R P, Facchetti A and Marks T J 2010 High-k organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors *Chem. Rev.* **110** 205–39
[23] Dong H L, Jiang L and Hu W P 2012 Interface engineering for high-performance organic field-effect transistors *Phys. Chem. Chem. Phys.* **14** 14165
[24] Kobayashi S, Nishikawa T, Takenobu T, Mori S, Shimoda T, Mitani T, Shimotani H, Yoshimoto N, Ogawa S and Iwasa Y 2004 Control of carrier density by self-assembled monolayers in organic field-effect transistors *Nat. Mater.* **3** 317
[25] Pernstich K P, Haas S, Oberhoff D, Goldmann C, Gundlach D J, Batlogg B, Rashid A N and Schitter G 2004 Threshold voltage shift in organic field effect transistors by dipole monolayers on the gate insulator *J. Appl. Phys.* **96** 6431
[26] Sajed F and Rutherglen C 2013 All-printed and transparent single walled carbon nanotube thin film transistor devices *Appl. Phys. Lett.* **103** 143303
[27] Zschieschang U, Ante F, Schlörholz M, Schmidt M, Kern K and Klauk H 2010 Mixed self-assembled monolayer gate dielectrics for continuous threshold voltage control in organic transistors and circuits *Adv. Mater.* **22** 4489
[28] Aghamohammadi M, Rödel R, Zschieschang U, Ocal C, Boschker H, Weitz R T, Barrena E and Klauk H 2015 Threshold-voltage shifts in organic transistors due to self-assembled monolayers at the dielectric: evidence for electronic coupling and dipolar effects *Appl. Mater. Interfaces* **7** 22775
[29] Wöbkenberg P H, Ball J, Kooistra F B, Hummelen J C, Leeuw D M, Bradley D D C and Anthopoulos T D 2008 Low-voltage organic transistors based on solution processed semiconductors and self-assembled monolayer gate dielectrics *Appl. Phys. Lett.* **93** 013303
[30] Klauk H, Zschieschang U, Pflaum J and Halik M 2007 Ultralow-power organic complementary circuits *Nature* **445** 745
[31] Arnold M S, Green A A, Hulvat J F, Stupp1 S I and Hersam M C 2006 Sorting carbon nanotubes by electronic

structure using density differentiation *Nat. Nanotechnol.* **1** 60–5
[32] Green A A and Hersam M C 2011 Nearly single-chirality single-walled carbon nanotubes produced via orthogonal iterative density gradient ultracentrifugation *Adv. Mater.* **23** 2185–90
[33] Cao Q, Xia M G, Kocabas C, Shim M, Rogers J A and Rotkin S V 2007 Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors *Appl. Phys. Lett.* **90** 023516
[34] Cao Q and Rogers J A 2009 Ultrathin films of single-walled carbon nanotubes for electronics and sensors: a review of fundamental and applied aspects *Adv. Mater.* **21** 29–53
[35] Zaumseil J 2015 Single-walled carbon nanotube networks for flexible and printed electronics *Semicond. Sci. Technol.* **30** 074001
[36] Jin S H, Islam A E, Kim T, Kim J-H, Alam M A and Rogers J A 2012 Sources of hysteresis in carbon nanotube field-effect transistors and their elimination via methylsiloxane encapsulants and optimized growth procedures *Adv. Funct. Mater.* **22** 2276–84
[37] Zhou X J, Park J-Y, Huang S M, Liu J and McEuen P L 2005 Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors *Phys. Rev. Lett.* **95** 146805
[38] Wang C, Zhang J L, Ryu K, Badmaev A, Arco L G D and Zhou C W 2009 Wafer-scale fabrication of separated carbon nanotube thin-film transistors for display applications *Nano Lett.* **9** 4285–91
[39] Chen P, Fu Y, Aminirad R, Wang C, Zhang J L, Wang K, Galatsis K and Zhou C W Fully printed separated carbon nanotube thin film transistor circuits and its application in organic light emitting diode control *Nano Lett.* **11** 5301–8
[40] Cao C Y, Andrews J B, Kumar A and Franklin A D 2016 Improving contact interfaces in fully printed carbon nanotube thin-film transistors *ACS Nano* **10** 5221–9
[41] Horowitz G and Delannoy P 1991 An analytical model for organic-based thin-film transistors *J. Appl. Phys.* **70** 469
[42] Cho K-H, Kang M-G, Jang H W, Shin H Y, Kang C-Y and Yoon S-J 2012 Significantly reduced leakage currents in organic thin film transistors with Mn-doped $Bi_2Ti_2O_7$ high-k gate dielectrics *Phys. Status Solidi* **6** 208–10
[43] Knipp D, Street R A, Völkel A and Ho J 2003 Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport *J. Appl. Phys.* **93** 347
[44] Fujii S, Tanaka T, Suga H, Naitoh Y, Minari T and Kataura H 2010 Site-selective deposition of single-wall carbon nanotubes by patterning self-assembled monolayer for application to thin-film transistors *Phys. Status Solidi* B **247** 2750–3
[45] Nirmalraj P N, Lyons P E, De S, Coleman J N and Boland J J 2009 Electrical connectivity in single-walled carbon nanotube networks *Nano Lett.* **9** 3890–5
[46] Garrett M P, Ivanov I N, Gerhardt R A, Puretzky A A and Geohegan D B 2010 Separation of junction and bundle resistance in single wall carbon nanotube percolation networks by impedance spectroscopy *Appl. Phys. Lett.* **97** 163105
[47] Fuhrer M S *et al* 2000 Crossed nanotube junctions *Science* **288** 494–7
[48] Jang Y, Cho J H, Kim D H, Park Y D, Hwang M and Cho K 2007 Effects of the permanent dipoles of self-assembled monolayer-treated insulator surfaces on the field-effect mobility of a pentacene thin-film transistor *Appl. Phys. Lett.* **90** 132104
[49] Goldmann C, Krellner C, Pernstich K P, Haas S, Gundlach D J and Batlogg B 2006 Determination of the interface trap density of rubrene single-crystal field-effect transistors and comparison to the bulk trap density *J. Appl. Phys.* **99** 034507
[50] Liu C, Xu Y, Li Y, Scheideler W and Minari T 2013 Critical impact of gate dielectric interfaces on the contact resistance of high-performance organic field-effect transistors *J. Phys. Chem.* C **117** 12337
[51] Halik M, Klauk H, Zschieschang U, Schmid G, Dehm C, Schütz M, Maisch S, Effenberger F, Brunnbauer M and Stellacci F 2004 Low-voltage organic transistors with an amorphous molecular gate dielectric *Nature* **431** 963–6
[52] Boulas C, Davidovits J V, Rondelez F and Vuillaume D 1996 Suppression of charge carrier tunneling through organic self-assembled monolayers *Phys. Rev. Lett.* **76** 4797–800
[53] Zojer K, Zojer E, Fernandez A F and Gruber M 2015 Impact of the capacitance of the dielectric on the contact resistance of organic thin-film transistors *Phys. Rev. Appl.* **4** 044002
[54] Jiang P, Li S-Y, Sugimura H and Takai O 2006 Pattern design in large area using octadecyltrichlorosilane self-assembled monolayers as resist material *Appl. Surf. Sci.* **252** 4230–5